RAGE™ XL
Graphics Controller Specifications

Technical Reference Manual
P/N: CHS-R3L-00-32

The information contained in this manual has been carefully checked and is believed to be entirely reliable. No responsibility is assumed for inaccuracies. ATI reserves the right to make changes at any time to improve design and supply the best product possible.

Record of Revisions

Release	Date
0.01-0.05 (previously 2.0-2.4)	Oct 1998 to Jan 1999
0.06	Mar 1999
0.07	Apr 1999
0.08	July 1999
1.00	Aug 1999
1.01	Nov 1999
2.00	Dec 1999
2.01	Mar 2000
2.02	May 2000
2.03	Oct 2000
3.00	Nov 2001
3.1	Sep 2003
3.2	Dec 2003
See Appendix B for revision history	

Related Manuals

RAGE XL series

- RAGE™ XL Register Reference Guide (RRG-G04300)
- RAGE™ XL Design Guide (DRS-D04300)

Table of Contents

Chapter 1: Introduction

1.1 About This Manual 1-1

1.2 ATI Component Part Number Legend 1-2

1.3 Conventions and Notations 1-3
- 1.3.1 Pin/Signal Names 1-3
- 1.3.2 Pin Types 1-3
- 1.3.3 Numeric Representation 1-4
- 1.3.4 Acronyms 1-4

Chapter 2: Overview

2.1 Feature Summary 2-1

2.2 General Features 2-1

2.3 RAGE XL Compatibility with other ATI Chips 2-2
- 2.3.1 Feature Compatibility with RAGE 128 VR 2-2
- 2.3.2 RAGE 128 Features Not Supported by RAGE XL 2-3
- 2.3.3 Feature Compatibility with the RAGE PRO 2-3

2.4 Features in Detail 2-5
- 2.4.1 Integrated TMDS 2-5
- 2.4.2 Digital Flat Panel Support 2-5
- 2.4.3 ACPI Power Management 2-6
- 2.4.4 Floating-Point Set-up Engine 2-6
- 2.4.5 Memory Support 2-6
- 2.4.6 DVD and Video Support 2-6
- 2.4.7 2D Acceleration 2-7
- 2.4.8 3D Acceleration 2-7
- 2.4.9 AMC Support 2-9

2.5 Software Features 2-10

Chapter 3: Pinout and Strap Descriptions

3.1 Pinout Summary 3-1

3.2 RAGE XL Pin Assignment: Top View 3-2
3.3 Host Bus Interface 3-3
3.4 Video Memory Interface 3-5
3.5 BIOS Memory Interface 3-5
3.5.1 BIOS EPROM Memory Interface Mapping 3-5
3.6 Multimedia Interface 3-6
3.6.1 Multimedia Interface Pinout 3-6
3.6.2 Standard Multimedia Configurations 3-7
3.7 TMDS Interface for Digital Flat Panels 3-7
3.8 CRT Monitor Interface 3-9
3.8.1 CRT Monitor Interface 3-9
3.8.2 Panel Control Interface 3-9
3.9 Miscellaneous Pins 3-10
3.9.1 Internal PLL and External Crystal Interface 3-10
3.9.2 Testing Pin 3-10
3.9.3 Clamping Pins 3-10
3.9.4 Power and Ground Pins 3-11
3.10 Strapping Options 3-13
3.10.1 Standard Boot-up Sequence 3-14
3.10.2 Configurations for Strap/BIOS Implementation 3-14
3.10.3 External Straps 3-16
3.10.4 Bus Configuration Settings 3-17
3.10.5 BIOS ROM Straps 3-17
3.10.6 Chip ID 3-17
3.11 Pinout Differences between RAGE XL and other ATI Chips 3-18
3.11.1 Function Support Differences between RAGE XL and RAGE 128 3-18
3.11.2 Pinout Differences between RAGE XL and RAGE 128 VR 3-18
3.11.3 Function Support Differences between RAGE XL and RAGE PRO 3-20
3.11.4 Power Differences between RAGE XL and RAGE PRO 3-21
3.11.5 Similarity and Differences between RAGE XL and RAGE Mobility 3-22

Chapter 4: Functional and Interfacing Descriptions

4.1 3D Graphics Coprocessor 4-2
4.2 2D Engine 4-3
4.3 IDCT Engine 4-4
4.4 Display System 4-5
4.4.1 Extended VGA Graphics Controller 4-5

4.4.2 CRT Controller (CRTC) 4-5
4.4.3 Display Controller 4-5
4.4.4 Hardware Cursor 4-5
4.4.5 Video Coprocessor 4-5
4.4.6 DVD Subpicture 4-6
4.4.7 Palette and CRT DAC 4-6
4.4.8 LCD Engine and Panel Interface 4-7
4.4.9 TMDS Interface 4-7
4.4.10 Ratiometric Expansion 4-8

4.5 Chip Power Management 4-8

4.6 Quadruple Clock Synthesizer 4-9

4.7 ATI Multimedia Channel (AMC) 4-9

4.8 Host Bus Interface 4-10
4.8.1 AGP Bus Interface 4-11
4.8.2 PCI Bus Interface 4-12

4.9 Memory Controller and Interface 4-13
4.9.1 Memory Configurations 4-13
4.9.2 Memory Interface Mapping 4-14
4.9.3 SDRAM Interface with 512Kx16x2 (16 Mbit) Devices (RAGE XL) 4-15
4.9.4 SGRAM Interface with 128x32x2 (8 Mbit) Devices 4-16
4.9.5 SGRAM Interface with 256x32x2 (16 Mbit) Devices 4-17
4.9.6 SGRAM Interface with 512Kx32x2 (32 Mbit) Devices 4-18
4.9.7 SDRAM Interface with 512Kx32x4 (64 Mbit) Devices 4-19
4.9.8 SO-DIMM Module Interface 4-20

4.10 EPROM Interface 4-21

4.11 Flash Memory Interface 4-22

4.12 General Purpose I/O Control 4-23

4.13 ATI Multimedia Channel 2.0 Interface (AMC) 4-23
4.13.1 DVS Mode 4-24
4.13.2 MPP Mode 4-25

4.14 Analog Output Section 4-26

Chapter 5: Timing Specifications

5.1 Bus Timings 5-1
5.1.1 Single Read/Write Cycle Timing 5-2
5.1.2 Disconnect On Burst Cycle - PCI Bus 5-3
5.1.3 Burst Access Timing - PCI 5-4
5.1.4 PCI Bus Master Operation 5-5

5.1.5 AGP Timing 5-7
5.1.6 Power-up and Reset Timing 5-9
5.2 Memory Timing 5-10
5.2.1 SDRAM/SGRAM Cycle Timing 5-11
5.2.2 Memory Controller Register Programming Examples 5-13
5.3 TMDS Timing 5-14
5.3.1 TMDS Transmission 5-14
5.3.2 TMDS Data/Clock Mapping 5-15

Chapter 6: Electrical and Physical Data

6.1 Electrical Characteristics 6-1
6.1.1 Maximum Rating Conditions 6-1
6.1.2 Recommended DC Operating Conditions 6-1
6.1.3 AC Characteristics 6-2
6.1.4 DC Characteristics 6-4
6.1.5 Input/Output Specifications 6-6
6.1.6 DAC Characteristics 6-8
6.1.7 Calculating RSET Resistance (DAC Interface) 6-9
6.1.8 Analog Output Specification 6-11
6.2 Thermal Characteristics 6-12
6.2.1 Maximum Ambient Temperature 6-12
6.2.2 Maximum Recommended Junction and Case Temperature 6-12
6.2.3 Board Power and Case Temperature Measurements 6-13
6.3 Physical Dimensions 6-14
6.4 Environmental Requirements 6-15
6.4.1 Storage Temperature 6-15
6.4.2 Relative Humidity 6-15

Chapter 7: Display Modes

7.1 2D Modes 7-1
7.2 Full Screen 3D Modes 7-3
7.3 DVD/Video Modes 7-4
7.3.1 Software MPEG Decoding 7-4
7.3.2 Hardware MPEG Decoding 7-5

Chapter 8: NAND Tree Implementation

8.1 Overview....8-2
8.2 NAND tree in RAGE XL....8-3
8.3 Test Modes....8-7
8.3.1 Board Test Modes....8-7
8.3.2 Other Test Modes....8-8
8.4 Testing Procedure....8-9
8.5 Pins Unused in NAND Tree....8-9

Appendix A: Pin Listings

A.1 Pins Sorted by Pin Name....A-2
A.1.1 Pins Sorted by Pin Number....A-6

Appendix B: Revision History

This page intentionally left blank.

Chapter 1
Introduction

1.1 About This Manual

This manual is part of a set of reference documents that provide information necessary to design the RAGE XL graphics controller into a graphics subsystem. These documents are listed on the back of the cover page.

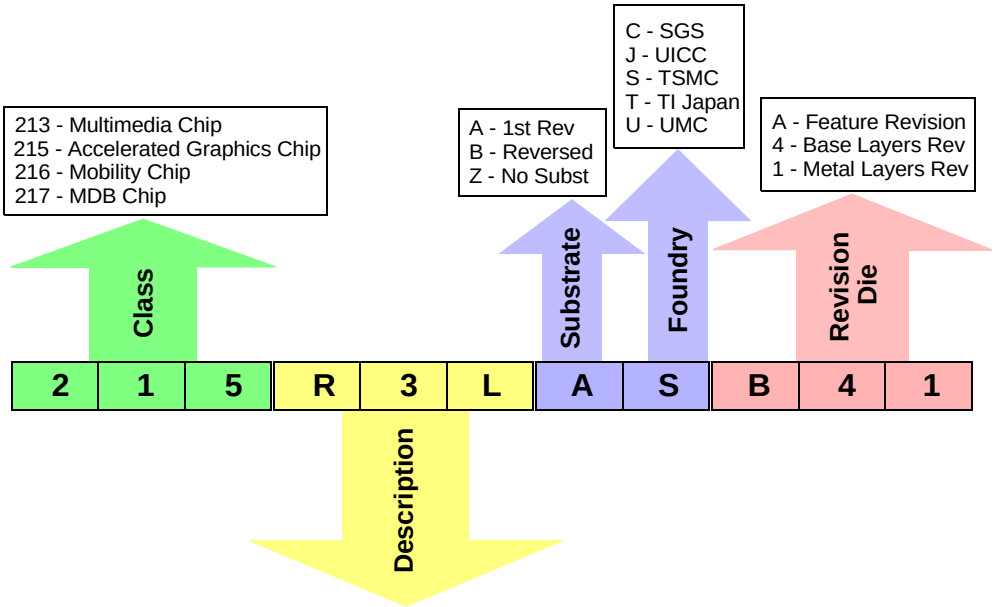
The electrical and thermal characteristics described in this document are specific to the RAGE XL manufactured using TSMC's 0.25µm process, which has voltages of 2.5V core, 3.3V PCI I/O (with 5.0V tolerance), 3.3V AGP, and 3.3V (LVTTL) memory interface. Please contact ATI to obtain information on how to support all of ATI's graphics controllers, steppings, and foundries in one PCB design.

Table 1-1 Summary of this Manual

Chapter	Description
1	Introduction to this manual.
2	Main features of RAGE XL.
3	Detailed description of the pins, the straps, and pinout differences for various graphics controllers.
4	Functions of the building blocks of the controller and the interface implementations.
5	Timing diagrams.
6	Electrical and physical characteristics.
7	Display modes supported.
A	Pin listing sorted by pin name and by pin number.
B	Revision History for this manual.

1.2 ATI Component Part Number Legend

The present manual is intended to cover RAGE XL parts 215R3LASBXX. The manual will be updated periodically to include latest component revisions and respective additional/changed specifications. The figure below shows how to read the coded information contained in a branded ATI component part number.



RAGE 128	RAGE MOBILITY	RAGE PRO
R4B - RAGE 128 VR, 272 BGA	L0S - L STN Enabled	R3B, R3C, R3D, R3E, R3P
R4G - 328/385 BGA (GL line)	L0T - L STN Disabled	
R4V - 329 BGA VR line (AGP 4X)	M0S - M STN Enabled	**RAGE IIC**
R4L- RAGE 128 PRO 2XL, 272 BGA	M0T - M STN Disabled	R2A, R2B, R2P, R2Q
R4F - RAGE 128 PRO 4X, 329 BGA	P0S - P STN Enabled	
R4U - RAGE 128 PRO 4XL, 329 BGA	P0T - P STN Disabled	**ImpacTV2**
		TV2, TV3, TV4, TV5
	RAGE LT PRO	
	LT2, LT3, LT4, LT5	**Others (pre-1997):**
		3D RAGE II/II+
	3D RAGE LT	GT1, GT2
	LG1, LT1	**ImpacTV**
		TB0, TB1
RAGE XL	**RAGE THEATER**	**ATI264**
R3L	RT1	VT2, VT3, CT

Figure 1-1. ATI Component Part Number Legend

1.3 Conventions and Notations

The following conventions are used for the pins described throughout this manual:

1.3.1 Pin/Signal Names

Mnemonics are used throughout this manual to represent pins and external strap resistors. For example, the Device Select pin and the Interrupt Enable external strap are represented by DEVSELb and ENINTb respectively.

All active-low signal names are identified by the suffix ‘b’ (e.g. BLANKb).

Pins may be identified by their *signal names* or ball references. The terms ***pin name*** and ***signal name*** are used indistinguishably in the industry; in this document pin name is used to allow for situations in which pins have different functions, and therfore signal names (e.g. pins in the multimedia group). For such multiplexed pins, the alternate name(s) will be adequately noted.

1.3.2 Pin Types

The assigned codes for the various pin types based on operational characteristics are listed in the table below.

Table 1-2 Pin Type Code

Code	Pin Type / Operational Characteristics
I	Input
O	Output
I/O	Bi-Directional
M	Multifunction
Pwr	Power
Gnd	Ground
A	Analog

1.3.3 Numeric Representation

Hexadecimal numbers are appended with “h” (Intel assembly-style notation) whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.

When the same pin name (except the following running integer) is used for pins that have identical functions (e.g. AD0, AD1), a short-hand notation is used to refer to all of them (i.e. AD[31:0] refers to AD0, AD1, ..., and AD31).

The above shorthand notation is not to be confused with that used to indicate bit occupation in a register. For example, SUBSYS_VEN_ID[15:0] refers to the Product Type Code field that occupies bit positions 0 through 15 within the 16-bit vendor ID register in PCI configuration space.

1.3.4 Acronyms

Standard acronyms used in the literature are presumed known and will not be explained. When in doubt, the reader can refer to the following table for a quick check. Less frequently used or ATI-specific acronyms will have the full definition alongside in parenthesis when they appear the first time in the document.

Table 1-3 Standard Acronyms

Acronym	Full Expression
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
AMC	ATI Multimedia Channel
BGA	Ball Grid Array
CRC	Cyclic Redundancy Check
DDC	Display Data Channel
DFP	Digital Flat Panel
DDR	Double Data Rate
DPMS	Display Power Management Signaling
DVS	Digital Video Stream
EPROM	Erasable Programmable Read Only Memory
FIFO	First In, First Out
I^2C	Bus Protocol (Philips Specification)
IDCT	Inverse Discrete Cosine Transform
LCD	Liquid Crystal Display

Table 1-3 Standard Acronyms (Continued)

Acronym	Full Expression
LOD	Level of Details (is referred to texture pixel selection)
MPP	Multimedia Peripheral Port
PEROM	Flash Programmable and Erasable Read Only Memory
PQFP	Plastic Quad Flat Pack
SDR	Single Data Rate
S/PDIF	Sony/Phillips Digital Interface
TFT	Thin Film Transister - active matrix
TMDS	Transmission Minimized Differential Signaling
UV	Chrominance (also CrCb). Corresponds to the color of a pixel.
VBI	Vertical Blank Interval
VFC	VESA Feature Connector
VIP	Video Interface Port
YUV	The method of video signal color encoding. Includes luma (Y, black and white component) and chroma (UV, color component)

This page intentionally left blank.

Chapter 2
Overview

2.1 Feature Summary

The RAGE XL graphics controller brings ATI's best of class 2D, 3D, and DVD performance to entry-level PCs and advanced Set-Top boxes. In addition, the RAGE XL is the first graphics controller to offer integrated TMDS transmitter support for Digital Flat Panel (DFP) monitors.

- **Outstanding 3D and 2D Performance** - the RAGE XL delivers superior 3D acceleration and comprehensive 3D support including a 1.2 million triangular/sec set-up engine, single pass trilinear filtering, six perspectively correct texturing modes, video texturing, Gouraud and specular shading, and a host of 3D special effects.
- **Built-in DVD Decoding** - ATI RAGE XL's integrated iDCT and Motion Compensation circuitry allow for Hardware DVD playback at full frame rate.
- **Set-Top Box Solution** - RAGE XL together with ATI RAGE Theatre (single chip video decoder and encoder) provides excellent set-top graphics and video subsystem. It supports 32-bit true color video/graphics alpha blending.
- **Integrated TMDS Flat Panel Support** - RAGE XL incorporates all the required logic to interface gluelessly with DFP monitors. This provides lowest cost DFP ready implementation through industry standard interfaces, while maintaining support for the existing VGA connector for legacy monitor support. This integrated TMDS transmitter meets VESA Plug-and-Play (P&D) digital transmission standard.
- **Full AGP 2X Support** - RAGE XL incorporates comprehensive support for Intel's AGP including 2x mode with Sideband addressing.
- **Full PCI Support** - RAGE XL supports both PCI 33MHz and PCI 66MHz operation.

2.2 General Features

- High integration results in a low cost, small footprint graphics subsystem ideal for motherboard designs.
- AGP version 1.0 support, including 2X mode, Sideband addressing.
- PCI version 2.2 with full bus mastering and scatter / gather support.
- Fully PC 99 compliant.
- Bi-endian support for compliance on a variety of processor platforms.

- Fast response to host commands:
  - Deep command FIFO.
  - 32-bit wide memory-mapped registers.
  - Programmable flat or paged memory model with linear frame buffer access.
- Triple 8-bit palette DAC with gamma correction for true WYSIWYG color. Pixel rates up to 230 MHz.
- Supports flexible memory configurations from 4 MB to 8 MB SDRAM/SGRAM at up to 125 MHz providing bandwidths of up to 1 GByte/sec across a 64-bit interface.
- Memory upgrade via industry standard SGRAM SO-DIMM for reduced board area and higher memory speeds.
- Supports 4MB 1Mx16 or 8MB 2Mx32 SDRAM at up to 125 MHz across a 32-bit interface for lowest cost configurations.
- DDC1 and DDC2B+ for plug and play monitors.
- Power management for full VESA DPMS and EPA Energy Star compliance.
- Integrated hardware diagnostic tests performed automatically upon initialization.
- High quality components through built-in SCAN, Iddq, CRC and chip diagnostics.
- Single chip solution in 0.25µ m, 2.5V CMOS technology, with multiple package options.
- Comprehensive HDKs, SDKs and utilities augmented by full engineering support.
- Complete local language support (contact ATI for current list).

2.3 RAGE XL Compatibility with other ATI Chips

For pin compatibility and differences see *"Pinout Differences between RAGE XL and other ATI Chips" on page 3-18*.

2.3.1 Feature Compatibility with RAGE 128 VR

- Supports 64-bit or 32-bit memory bus in 2MB, 4MB, 8MB SDRAM or SGRAM configurations (DDR is not supported).
  - Up to 125 MHz SDR 64-bit memory bus.
  - Up to 143 MHz SDR 32-bit memory bus.
- Supports hardware-accelerated DVD playback at full frame rates with no additional cost via integrated IDCT and Motion Compensation circuitry.

- Comprehensive support for Accelerated Graphics Port (AGP) including 2X mode, Sideband Addressing and AGP Texturing.
- Superior 3D acceleration and comprehensive 3D support which includes:
  - Triangle set-up engine.
  - Single-pass tri-linear filtering.
  - Six perspectively correct texturing modes.
  - Video texturing.
  - Gouraud and specular shading.
  - A host of 3D special effects video enhancements.
  - Floating point setup engine rated at 1.2 million triangles/sec.
- Integrated 230 MHz DAC.
- Increased command FIFO size — 512 entries.
- Supports ratiometric expansion.
- Supports RAGE THEATER and ImpacTV2 chips.

2.3.2 RAGE 128 Features Not Supported by RAGE XL

- Double-buffered bus-master command tables for MPEG writes through MPP Port.
- Bus-mastered MPP reads.
- MPP enhanced mode. (MPP and TVout will be exactly the same as the RAGE IIC.)
- VIP port.
- Dedicated I^2C controller pins.

2.3.3 Feature Compatibility with the RAGE PRO

RAGE XL has these same features as RAGE PRO:

- 32-bit PCI bus, 3.3V only (5V tol.), with bus mastering support.
- AGP-66 with 1X transfer and AGP-133 with 2X transfer. Both with full sideband addressing only and no support for PIPE#.
- ROM or Flash RAM video BIOS.
- Multimedia.

- Independent I^2C interface.
- RGB CRT monitor with DDC or AppleSense lines.
- Independent ring and core supplies to enable Iddq testing, NAND tree and internal scan chain.

2.4 Features in Detail

2.4.1 Integrated TMDS

- Integrated TMDS transmitter complying to VESA Plug-and-Display (P & D) digital transmission standard.
- TMDS support for both direct-coupling and capacitor-coupling.

2.4.2 Digital Flat Panel Support

- Glueless support for industry Digital Flat Panel (20-pin MDR).
- Universal panel interface that supports the followings:
  - Color TFT panel up to 1024x780 resolution, up to 24 bit per pixel, single pixel per clock.
  - 2/4 levels of frame modulation can be done on 18-bit TFT panels.
  - Hardware Z-buffer support with TFT panels.
- Ratiometric Expansion in both VGA Graphics Modes and Accelerated Graphics Modes. Display modes with resolutions lower than the LCD panel resolution can be ratiometrically expanded to fill the whole screen. 2- tap horizontal and vertical filtering to improve both text and graphics image quality. Maximum source resolution support with vertical filtering:
  - Horizontal: 1024 24bpp.
  - Vertical: no limit. There is no limit on source resolution if the vertical filtering is disabled.
- Monitor detection through hot plugging support.
- Flat Panel Power Management.
  - Standby/Suspend registers for software Power Management support.
- DDC support for LCD monitors. Dedicated I/O pins are available to support DDC on LCD monitor applications.
- Variable Blink Rate Support. Different panels have different response times. Variable blink rate support allows the blinking character/cursor to be seen clearly.
- Backlight Modulation. Pulse Width Modulation (up to 256 levels) for backlight on/off signal to control the brightness of the display.

2.4.3 ACPI Power Management

- Advanced Configuration and Power Interface (ACPI) with On, Standby, Suspend and Off modes.
- Register and Timer modes for hardware and software power management.
- Dynamic clock switching.
- Self-refresh SDRAM/SGRAM in Suspend mode.

2.4.4 Floating-Point Set-up Engine

This floating-point set-up engine is capable of processing up to 1.2 million triangles per second. By off-loading the set-up function from the CPU, allowing it to focus on 3D geometry and lighting transformations, RAGE XL dramatically improves the performance of the entire 3D pipeline.

Compared with competing first generation set-up engines which only accept fixed-point parameters, requiring the CPU to perform float-to-fixed conversions that can take up to 100 CPU clocks, ATI's floating point architecture opens the door to the highest level of 3D performance.

2.4.5 Memory Support

- Single data rate (SDR) SGRAM/SDRAM up to 125 MHz across a 64-bit interface (1.06 GB/s).
- Support only LVTTL.

2.4.6 DVD and Video Support

- Hardware DVD decode via integrated motion compensation and IDCT circuitry for full frame rate DVD playback.
- Support for hardware DVD subpicture decoder.
- 4-tap horizontal and 2-tap vertical high quality DVD video scaler, providing smooth images without the jagged edges ("jaggies") common to video products. The scaler provides true color video display, independent of the graphics mode used.
- Front and back end scalers support multi-stream video for video conferencing and other applications.

- YUV direct interface to RAGE THEATER without requiring data to be converted to RGB.
- Enhanced line buffer allows vertical filtering of native MPEG-2 size (720x480) images.
- Special filter circuitry eliminates video artifacts caused by displaying interlaced video on non-interlaced displays.
- Bi-directional bus mastering engine with full YUV planar mode support for superior MPEG-2 and video conferencing.
- Hardware mirroring for flipping video images in video conferencing systems.
- Supports graphics and video keying for effective overlay of video and graphics.
- Smooth video scaling and enhanced YUV to RGB color space conversion for full-screen / full-speed video playback. YUV to RGB color space converter with support for both packed and planar YUV:
  - YUV422, YUV410, YUV420.
  - RGB32, RGB16/15.
- ATI Multimedia Channel (AMC) video input port, and support for high quality NTSC and PAL TV-out with the ATI ImpacTV2 or RAGE THEATER chips.
- Support 4-bit video and graphics alpha blending ARGB8888 in YUV space for TV out or RGB space for DAC(CRT)/DFP.

2.4.7 2D Acceleration

- Hardware acceleration of Bitblt, Line Draw, Polygon / Rectangle Fill, Bit Masking, Monochrome Expansion, Panning/Scrolling, Scissoring, full ROP support and hardware cursor (up to 64x64x2).
- Game acceleration including support for Microsoft's DirectDraw: Double Buffering, Virtual Sprites, Transparent Blit, Masked Blit and Context Chaining.
- Acceleration in 8/16/24/32 bpp modes.

2.4.8 3D Acceleration

- Integrated 1 million triangle/s set-up engine reduces CPU and bus bandwidth requirements and dramatically improves performance of small 3D primitives
- 4K on-chip texture cache dramatically improves large triangle performance.

- Complete 3D primitive support: points, lines, triangles, lists, strips and quadrilaterals and BLTs with Z compare.
- Comprehensive enhanced 3D feature set:
  - Full screen or window double buffering for smooth animation.
  - Hidden surface removal using 16-bit Z-buffering.
  - Z-based fog.
  - Fog table integration.
  - Edge anti-aliasing.
  - Sub-pixel and sub-texel accuracy.
  - Gouraud and specular shaded polygons.
  - Bi-linear interpolation of texture alpha.
  - Modulate alpha function.
  - Composite alpha modulate.
  - Perspectively correct mip-mapped texturing with chroma-key support.
  - Support for single pass bi- and tri-linear texture filtering, vastly improving bi- and tri-linear performance.
  - Full support of Direct3D texture lighting.
  - Texture compositing.
  - Special effects such as complete alpha blending, fog, video textures, texture lighting, reflections, shadows, spotlights, Level of Details (LOD) biasing and texture morphing.
  - Dithering support in 16bpp for near 24bpp quality in less memory.
  - Texture compression of up to 8:1 using vector quantization.
- Extensive 3D mode support:
  - Draw in RGBA32, RGBA16, and RGB16.
  - Texture map modes: RGBA32, RGBA16, RGB16, RGB8, ARGB4444, and YUV444.
  - Compressed texture modes: YUV422, CLUT4 (CI4), CLUT8 (CI8), and VQ.

2.4.9 AMC Support

The 8-bit, bi-directional video port allows direct connection to popular video upgrades such as:

- Video capture / video conferencing.
- Hardware MPEG-2 / DVD player.
- TV Tuner with Intercast support.
- Interface to ATI's ImpacTV or RAGE THEATER chip.

2.5 Software Features

- Register-compatible with VGA standards, BIOS-compatible with VESA Super VGA.
- Full-featured, yet simple Windows utilities:
  - ATI DeskTop supports panning and scrolling across a virtual workspace;
  - Calibration utility for WYSIWYG color.
- Drivers meet Microsoft's rigorous WHQL criteria and are suitable for systems which bear the "Designed for WindowsNT and Windows98" logo.

Table 2-1 Software Support

Software Support	DOS	Win 3.x	Win 9x	NT 3.51	NT 4.0	Win 2000	Mac OS	OS/2
2D Software Support[1]								
Accelerated driver support	VESA[2]	●	●	●	●	●	●[7]	●
AutoCAD/ MicroStation	●							
Video Software Support								
Microsoft DirectDraw			●		●	●		
Microsoft ActiveMovie/ DirectShow			●			●		
MPEG-1 software playback			●		●	●		
DVD/MPEG-2 software playback			●			●		
QuickTime acceleration							●	
3D Software Support								
Microsoft Direct3D			●			●		
QuickDraw 3D RAVE							●	
OpenGL			●[3]		●[3]	●[6]		
ATI 3D CIF[4]	●							
AGP			●		●[5]	●		

Notes:

1 - Additional drivers availability from 3rd parties (including SCO and UNIXWARE).

2 - Direct BIOS support.

3 - OpenGL ICD.

4 - ATI's 3D API for the 3D RAGE family.

5 - NT 4.0 Service Pack 3 supports AGP devices, but does not provide support for AGP Texturing.

6 - Dependent on NT 5.0 release date.

7 - Includes QuickDraw support.

Chapter 3
Pinout and Strap Descriptions

This chapter describes pin and strap assignments for RAGE XL. It also includes a section on pin compatibility between RAGE XL and other ATI controller chips.

3.1 Pinout Summary

Table 3-1 Pin Summary by Functional Group

Functional Group	RAGE XL BGA-Type Package
Clamps	2
Core Ground (VSSC)	4
Core Power (VDDC)	5
CRT Monitor Interface	9
Crystal and PLL	4
Host Bus Interface	62
I/O Ground (VSSR)	16
I/O Power (VDDR)+VREF	9
Memory Interface	93
Monitor Panel Control	7
Multimedia Interface	23
No Connection	15
PCI/AGP Ground (VSSP)	3
PCI/AGP Power (VDDP)	4
Test	1
TMDS Interface	15
Pin Count:	**272**

3.2 RAGE XL Pin Assignment: Top View

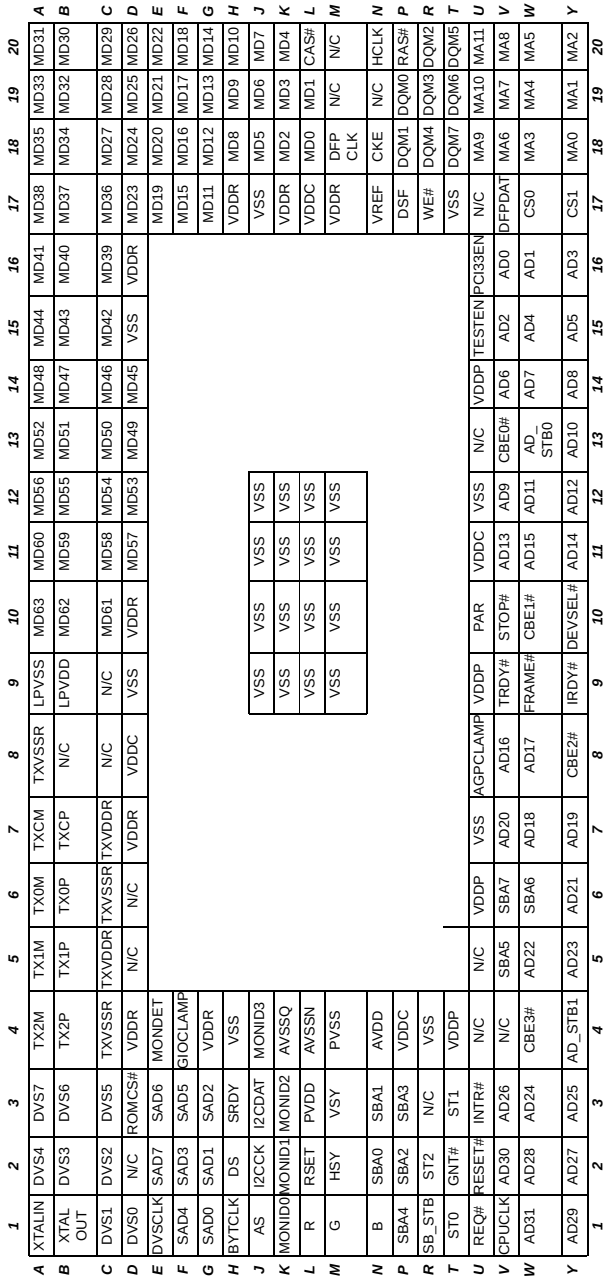


Figure 3-1 RAGE XL Top View

3.3 Host Bus Interface

RAGE XL supports PCI 33MHz, PCI 66MHz, AGP 1X, or AGP 2X buses.

Table 3-2 AGP/PCI Bus Interface

Signal Name	I/0 Type	Description
AD[31:0]	I/O	System Address
AD_STB[1:0]	I/O	Address Strobe (for AGP-133 support)
CBE[3:0]#	I/O	Bus Command or Byte Enable
CPUCLK	I	Bus Clock
D[31:0]	I/O	Data
DEVSEL#	I/O	Device Select When driven active “low”, indicates that the graphics controller has decoded its address. Not used by AGP.
FRAME#	I/O	Frame Driven by the current bus master to indicate the beginning and duration of an access.
GNT#	I	Grant Signal from Arbiter Indicates to the agent that a bus access has been granted.
INTR#	O	Interrupt Request Level triggered. Active “low” by default.
IRDY#	I/O	Initiator Ready Indicates that the bus master is able to complete the current data phase of the transaction.
PAR	O	Parity Even parity used (expand on parity detection).
PCI33EN	I	Enable PCI 33MHz Mode
REQ#	O	Request Signal to Arbiter Indicates to the systems’ chip set that there is request for bus master cycle.
RESET#	I	PCI Reset
SBA[6:0]	O	Sideband Address Port (for AGP-133 support)
SBA7 / IDSEL	I/O	In AGP mode, AGP Sideband Address Port Bit 7 **or** In PCI mode, PCI Initialization Device Select
SB_STB	O	Sideband Strobe (for AGP-133 support)
ST[2:0]	I	Status Bus (for AGP support)
STOP#	I/O	Stop Indicates the current target is requesting the master to stop the current transaction. Not used by AGP.

Table 3-2 AGP/PCI Bus Interface (Continued)

Signal Name	I/0 Type	Description
TRDY#	I/O	Target Ready Indicates the target agent is able to complete the current data phase of the transaction.

NOTE:
In PCI mode, IDSEL will be supported through the SBA7 pin. In AGP mode, IDSEL will be multiplexed through pin AD16 or AD17 depending on the setting of the “IDSEL#’ strap.
For PCI implementations, leave all unused AGP-only pins as no-connect (i.e. open).
Total number of pins in this functional group is 62.

Table 3-3 Host Bus Interface by Bus Type

Signal Name	Bus Type			
	PCI 33 MHz PCI33EN = 1	PCI 66 MHz PCI33EN = 0	AGP 66 MHz PCI33EN = 0	AGP 133 MHz PCI33EN = 0
AD[31:0]	AD[31:0]	AD[31:0]	AD[31:0]	AD[31:0]
AD_STB[1:0]	-	-	-	ADST[1:0]#
CBE[3:0]#	CBE[3:0]#	CBE[3:0]#	CBE[3:0]#	CBE[3:0]#
CPUCLK	CPUCLK	CPUCLK	CPUCLK	CPUCLK
DEVSEL#	DEVSEL#	DEVSEL#	DEVSEL#	DEVSEL#
FRAME#	FRAME#	FRAME#	FRAME#	FRAME#
GNT#	GNT#	GNT#	GNT#	GNT#
INTR#	INTR#	INTR#	INTR#	INTR#
IRDY	IRDY	IRDY	IRDY	IRDY
PAR	PAR	PAR	PAR	PAR
REQ#	REQ#	REQ#	REQ#	REQ#
RESET#	RESET#	RESET#	RESET#	RESET#
SBA[6:0]	-	-	SBA[6:0]	SBA[6:0]
SBA7	IDSEL	IDSEL	SBA7	SBA7
SB_STB	-	-	-	SBST#
ST[2:0]	-	-	ST[2:0]	ST[2:0]
STOP#	STOP#	STOP#	STOP#	STOP#
TRDY#	TRDY#	TRDY#	TRDY#	TRDY#
Number of Pins:	**48**	**48**	**58**	**62**

3.4 Video Memory Interface

Table 3-4 Video Memory Interface

Signal Name	I/O Type	Description
CAS#	I/O	Column Address Select
CKE	I/O	Clock Enable for Memory
CS[1:0]	I/O	Chip Select for Memory
DQM[7:0]	I/O	Memory Data Byte Mask
DSF	I/O	Memory special function enable for all supported SGRAM memory devices with the exception of the SDRAM 512Kx32x4 memory device. (Please refer to *Table 4-3* for more details on Memory Address Mapping).
HCLK	I/O	Memory Clock
MA[11:0]	I/O	Memory Address Bus
MD[31:0]	I/O	Memory Data Bus
MD[63:32]	I/O	Memory Data Bus
RAS#	I/O	Row Address Select
ROMCS#	I/O	Chip Select for ROM (video BIOS)
WE#	I/O	Write Enable

Note: Total number of pins in this functional group is 93.

3.5 BIOS Memory Interface

3.5.1 BIOS EPROM Memory Interface Mapping

Table 3-5 BIOS EPROM Memory Mapping

Memory Data Pins	EPROM Interface		Flash EPROM Interface	
	64KB	128KB	64KB	128KB
MD[47:32]	A[15:0]	A[15:0]	A[15:0]	A[15:0]
MD[48]	-	A[16]	-	A[16]
MD[50]	-	-	WE#	WE#
MD[51]	OE#	OE#	OE#	OE#
MD[63:56]	D[7:0]			
ROMCS#	CS#	CS#	CS#	CS#

3.6 Multimedia Interface

3.6.1 Multimedia Interface Pinout

Table 3-6 AMC Pinout

Signal Name	Pin Type	Description
AS	I/O	MPP Address Strobe
BYTECLK	I/O	BYTECLK (for ImpacTV)
DS	I/O	MPP Data Strobe
DVS[7:0]	I	DVS Data In
DVSCLK	I	DVS Clock In
I2CCK	O	I^2C Clock Out
I2CDAT	I/O	I^2C Data In/Out
SAD[7:0]	I/O	Address / data for MPP[7:0] TV out data for ImpacTV interface.
SRDY / IRQ	I/O	MPP Ready / Interrupt

Note: Total number of pins in this functional group is 23.

3.6.2 Standard Multimedia Configurations

Table 3-7 Standard Multimedia Configurations

Signal Name	MPP port	ITU-601 Video Capture Port	DVS port	I²C	ImpactTV or Rage Theater	GP Register Bit
DVS(7:0)		I601DAT(7:0)	YUV(7:0)			
DVSCLK		I601CLK	CLK			
SAD(7:0)	SAD(7:0)	*	*	*	Pixel Data	GPIO(7:0)
AS	SIOW (DS)	*	*	*	*	GPIO(8)
DS	SIOR (AS)	*	*	*	*	GPIO(9)
SRDY	SRDY/IRQ	*	*	*	*	GPIO(10)
BYTECLK	*	*	*	*	Pixel Clock	GPIO(11)
I2CDAT	*	*	*	I²CDATA	*	GPIO(12)
I2CCK	*	*	*	I²CCLK	*	GPIO(13)
MONID(3:0)	*	*	*	*	*	GPIO(17:14)
DFPCLK	*	iHREF	*	*	*	
DFPDAT	*	iVSYNC	*	*	*	

Notes:
- Any extra pins not used (*) in a particular mode can be used as general purpose I/O pins (GPIO)
- GPIO(17:14) are mapped from LT_GIO register (offset 0_2A index 7) – please refer to Rage XL Register Specification
- iHREF and iVSYNC are used as inputs for ITU video capture, and their directions are controlled by TMDS register TEST_IO Index 28. **TMDS and ITU-601 features are mutually exclusive in B41 revision**.

3.7 TMDS Interface for Digital Flat Panels

Table 3-8 TMDS Interface

Signal Name	Pin Type	Description
LPVDD	I	TMDS PLL Power
LPVSS	O	TMDS PLL Ground
TX0M	O	TX0- TMDS (-) Differential Transmitter Output For Blue
TX0P	O	TX0+ TMDS (+) Differential Transmitter Output For Blue

Table 3-8 TMDS Interface (Continued)

Signal Name	Pin Type	Description
TX1M	O	TX1- TMDS (-) Differential Transmitter Output For Green
TX1P	O	TX1+ TMDS (+) Differential Transmitter Output For Green
TX2M	O	TX2- TMDS (-) Differential Transmitter Output For Red
TX2P	O	TX2+ TMDS (+) Differential Transmitter Output For Red
TXCM	O	TXC- TMDS (-) Differential Transmitter Output Clock
TXCP	O	TXC+ TMDS (+) Differential Transmitter Output Clock
TXVDDR (X2)	I	TMDS Transmitter Power
TXVSSR (X3)	O	TMDS Transmitter Ground

Note: Total number of pins in this functional group is 15.

The TMDS transmitter encodes the 8-bit LPIXD data into the 10-bit PIXD10B encoded word. Special sync characters are used to delimit valid pixel data as shown below in TMDS out-of-band patterns table. For more details, refer to the VESA Plug-and-Display standard specifications.

Table 3-9 TMDS Sync Character Table

HSYNC PLL_SYNC CTL2	VSYNC PLL_SYNC CTL3	d0	d1	d2	d3	d4	d5	d6	d7	d8	d9
0	0	0	0	1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	1	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1	0
1	1	1	1	0	1	0	1	0	1	0	1

3.8 CRT Monitor Interface

3.8.1 CRT Monitor Interface

Table 3-10 CRT Monitor Interface

Signal Name	Pin Type	Description
AVDD	A-I	DAC VDD (2.5V)
AVSSQ	A-O	DAC VSS Quite ground used for bandgap.
AVSSN	A-O	DAC VSS noisy ground used as a current dump.
B	A-O	Blue Signal for Monitor
G	A-O	Green Signal for Monitor
HSYNC	O	Horizontal Sync Output
R	A-O	Red Signal for Monitor
RSET	A-O	Internal Reference
VSYNC	O	Vertical Sync Output

Note: Total number of pins in this functional group is 9.

3.8.2 Panel Control Interface

Table 3-11 Panel Control Interface

Signal Name	Pin Type	Description
DFPCLK	I/O	Flat Panel Clock
DFPDAT	I/O	Flat Panel Data
MONDET	I	Hot Plug Monitor Detect
MONID[0]	I/O	Flat Panel DIGON
MONID[2:1]	I/O	DDC Monitor Sensing
MONID[3]	I/O	Apple Monitor Sensing/Flat Panel BLON

Note: Total number of pins in this functional group is 7.

3.9 Miscellaneous Pins

3.9.1 Internal PLL and External Crystal Interface

Table 3-12 External Crystal Interface Pins

Signal Name	Pin Type	Description
PVDD	A-I	Phase Lock Loop Power (2.5 V)
PVSS	A-O	Phase Lock Loop Ground
XTALIN	I	PLL Reference Clock -OR- MXCLK Source 4
XTALOUT	O	PLL Reference Clock

Note: Total number of pins in this functional group is 4.

3.9.2 Testing Pin

Table 3-13 Testing Pin

Pin Name	Pin Type	Description
TESTEN	I	Test Enable for test mode

Note: Total number of pins in this functional group is 1.

3.9.3 Clamping Pins

Table 3-14 Clamping Pins

Pin Name	Pin Type	Description
AGPCLAMP[a]	I	Clamp for 5V Tolerance / Signal integrity on PCI
GIOCLAMP[b]	I	Clamp for 5V Tolerance / Signal integrity on Memory and GIOs

Notes:
a) AGPCLAMP pin should be connected to 3.3V power supply in AGP system and PCI system with 3.3V signalling. In a PCI system with 5.0V signaling, this pin should be connected to 5.0V.

b) If the GIO signal is 3.3V, GIOCLAMP pin should be connected to 3.3V power supply. If the GIO signal is 5.0V, this pin should be connected to 5.0V power supply.

3.9.4 Power and Ground Pins

Table 3-15 TMDS Power Pins

Signal Name	Pin Type	Description
LPVDD	I	TMDS PLL Power
LPVSS	O	TMDS PLL Ground
TXVDDR (X2)	I	TMDS Transmitter Power
TXVSSR (X3)	O	TMDS Transmitter Ground

Table 3-16 Power and Ground Pins

Signal Name	Pin Type	Description
AVDD	I	Analog DAC Power - 2.5V
AVSSN	O	Analog DAC Ground
AVSSQ	O	Analog DAC Ground
PVDD	I	PLL Power - 2.5V
PVSS	O	PLL Ground
VDDC	I	Core Power - 2.5V For the graphics controller.
VDDP	I	PCI/AGP Power - 3.3V For PCI or AGP interface.
VDDR	I	I/O Power - 3.3V For memory and multimedia.
VSS	O	Ground

Table 3-17 Power and Ground Pins Count

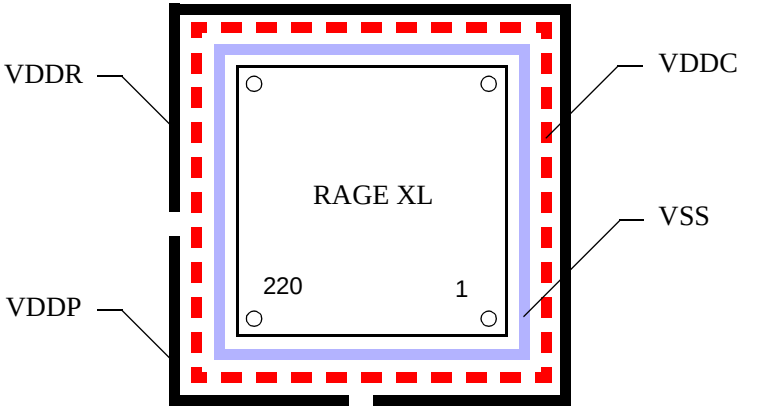
Signal Name	Number of Pins
VDDC	4
VDDP	4
VDDR	9 (8+VREF)
VSS	48
AVSSQ	1
AVSSN	1
AVDD	1
LPVDD	1
LPVSS	1

Table 3-17 Power and Ground Pins Count (Continued)

Signal Name	Number of Pins
TXVDDR	2
TXVSSR	3

Power and Ground Rings for the RAGE XL

Top View



VDDC = 2.5V ± 5%
VDDP = 3.3V ± 10%
VDDR = 3.3V ± 10%

Figure 3-2 Power and Ground Rings

3.10 Strapping Options

RAGE XL uses two groups of straps:

- External Straps
  These straps are located on the Memory Address pins and are required[1] for proper initialization of the chip before bus cycles can occur.
- BIOS ROM Straps
  These straps are stored in BIOS ROM.

Note 1: Clarification of the first bullet:
Although RAGE XL contains internal pull-up and pull-down resistors, external pull-up/pull-down resistor straps are required to ensure proper initialization of the ASIC for all implementations.

3.10.1 Standard Boot-up Sequence

The boot-up sequence is as follows:

1. PCI reset is asserted.

2. External straps are fed into the chip.

3. PCI reset is deasserted.

4. External straps are flopped in.

5. ROM state machine begins to read “ROM based straps”.

6. PCI may begin its first transfer - taken but not serviced yet.
   Note: The first PCI transfer to the Rage XL chip must not be a WRITE cycle. Since the BIOS straps have not yet been fully latched, the results of a WRITE cycle at this time is undefined. It is recommended that the first transfer to the Rage XL be a READ cycle, preferably a PCI CFG SPACE READ cycle. The second PCI transfer to the Rage XL chip can be a cycle of any type.

7. Finish reading the straps and begin processing PCI request.

8. Copy ROM into system memory.

3.10.2 Configurations for Strap/BIOS Implementation

There are three configurations for strap and BIOS implementation.

Configuration #1: For add-in card designs

For this case, there is an access to a local BIOS EPROM (ADD_IN_CARD strap installed). The sequence of events at power up is suggested as follows:

1. System reset goes active and the strap latches are opened to read pin level straps.

2. Reset is removed and shortly after the strap latches are closed.

3. A local routine between the controller and the EPROM is initiated to read the additional straps stored in the EPROM.

4. The first PCI configuration cycle is initiated and the EPROM is read and stored in the system memory.

5. Standard operations can begin.

The ROM state machine implemented in the Rage XL will read in all the "ROM based straps" right after PCI reset is deasserted. The ROM should be able to take PCI cycle but not respond to it until all straps are read. There is a total of 5 bytes worth of "ROM based straps" which are stored at byte location 0x4A through 0x4E within the lower 32KB space in the ROM/FLASHROM. The first four bytes contain **subsys_venid**[15:0] and **subsys_id**[15:0] and the fifth byte contains **chg_id** (change id) which is only 1 bit wide. The other 7 bits are reserved for future use.

Configuration #2: For motherboard designs

For this case, the video BIOS is stored in the system BIOS EPROM or flash ROM (ADD_IN_CARD strap not installed). The sequence of events at power up is suggested as follows:

1. System reset goes active and the strap latches are opened to read pin level straps.

2. Reset is removed, and, shortly after, the strap latches are closed.

3. The first PCI config cycle is initiated, and the additional straps stored in the video BIOS are written into the controller.

4. Standard operations can begin.

The System BIOS will be responsible for loading the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID through an aliased address in the reserved configuration space. The reason for writing through an aliased address (16#4c) is that the config location 16#2c is read only. Any writes to this location 16#4c will change the content of the SUBSYSTEM VENDOR ID at 16#2c. The Chg_id strap is not required on a motherboard implementation.

If neither the System BIOS nor the add-in card video BIOS supply the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID, the values of the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID are defaulted to chip-id and 0x1002 h (vendor-id) respectively inside the chip.

Configuration #3: Combination of Configurations #1 and #2

This case is a combination of one graphics controller located on the add-in card and another one located on the mother board.

The system BIOS will take care of the graphics device on the motherboard like in case #2, while the chip on the add-in board will be taken care of like in case #1. Since the ROM state machine from the graphics chip will read the "ROM based straps" independently of the video bios, the case where the OS is not reading the add-in card's video BIOS should be covered.

3.10.3 External Straps

Table 3-18 External Straps

Strap Name	Functions	Default	Pin Name
ADD_IN_CARD	0 - Don't Read BIOS straps 1 - Read BIOS straps	0	ROMCS#
BUS_CLK_SEL	Refer to *Table 3-19Bus Configuration Settings on page 3-17*.	0	MA0
AGPSKEW[1:0]	Adjust skew between refclk and pllclk	0	MA[2:1]
X1CLK_SKEW	Adjust skew between x1clk and x2clk.	0	MA[4:3]
ID_DISABLE	0 - Normal 1 - IDSEL disabled. Chip won't respond to config cycles	0	MA5
BUS_TYPE	Refer to *Table 3-19Bus Configuration Settings on page 3-17*.	0	MA6
VGA_DISABLE	0 - VGA is enabled 1 - VGA is disabled	0	MA7
ENINT#	0 - Interrupt pin enabled 1 - Interrupt pin disabled	0	MA8
IDSEL	In AGP mode, determines whether pin AD16 or AD17 is used as IDSEL: 0 = AD16 1 = AD17	0	MA9
AGP_VCO_GAIN[1:0]	VCO gain for AGP PLL	0	MA[11:10]

3.10.4 Bus Configuration Settings

Table 3-19 Bus Configuration Settings

Host Bus Type	BUS_CLK_SEL strap	BUS_TYPE strap	PCI33EN pin
AGP 1X, 2X	0	0	0
PCI 33 MHz, 3.3V Signaling	1	0	1
PCI 33 MHz, 5.0V Signaling	1	1	1
PCI 66 MHz	0	1	0

Note: For those straps that must be set on the board, the use of 10 KΩ resistors is recommended for pull-ups to power (3.3V) or pull-downs to ground.

3.10.5 BIOS ROM Straps

Table 3-20 BIOS ROM Straps

Strap	ROM Location (Byte Adr)	Description	Default
subsys_ven_id[15:0]	0x4B to 0x4A	Special class of config id required for WIN9x. For add-in card designs, video ROM writes in the id **after** PCI reset. For motherboard designs, system ROM writes in the id **before** the enumeration cycle is initiated.	1002h
subsys_id[15:0]	0x4D to 0x4C	Same as subsys_ven_id	chip_id (see *Table 3-21* below)

3.10.6 Chip ID

Table 3-21 Chip ID

Bus Interface	RAGE XL ChipID PKGBGA# = 0
AGP 1X, 2X	GM (474Dh)
PCI 33 MHz	GR (4752h)
PCI 66 MHz	GO (474Fh)

3.11 Pinout Differences between RAGE XL and other ATI Chips

With a few exceptions, RAGE XL is pin-compatible with RAGE 128 VR (272-pin BGA package) and RAGE PRO Turbo (272-pin BGA package). The exceptions are detailed below.

3.11.1 Function Support Differences between RAGE XL and RAGE 128

Table 3-22 Function Support Differences: RAGE XL vs. RAGE 128

Function	RAGE 128	RAGE XL
BIOS EPROM	BIOS EPROM interface through MPP port	BIOS EPROM interface through MD bus, identical to RAGE PRO
CS	Supports up to four memory banks with CS2 and CS3	Supports only up to two memory banks, since there are no CS2, and CS3 pins
DDR	Supports DDR and SDR memory	Only supports SDR
Power	Separate DDR I/O power rails for 2.5V, 3.3V, VDDR1 and VDDR2	Single 3.3V VDDR IO power rail
Straps	Straps are on MPP bus	Straps are on MA bus
TMDS	Does not support TMDS Panel Interface	Supports Panel Interface, including MONDET and Panel DDC
VIP/ZV	Supports VIP, secondary MPP and ZV port	Only supports primary MPP and ITU-601 (in revision B41 only)

3.11.2 Pinout Differences between RAGE XL and RAGE 128 VR

RAGE XL and RAGE 128 VR (272-pin BGA-type package) have identical pinouts with the following exceptions.

Table 3-23 Pinout Differences: RAGE XL vs. RAGE 128 VR

RAGE XL and RAGE 128 VR Pin Reference	RAGE 128 VR Signal Name	RAGE XL Signal Name
A4	Memory Data / MPP2 Data / LCD Interface Data	TX2M
A5	Memory Data / MPP2 Data / LCD Interface Data	TX1M
A6	Memory Data / MPP2 Data / LCD Interface Data	TX0M
A7	Memory Data / MPP2 Data / LCD Interface Data	TXCM
A8	Memory Data / MPP2 Data / LCD Interface Data	TXVSSR

Table 3-23 Pinout Differences: RAGE XL vs. RAGE 128 VR (Continued)

RAGE XL and RAGE 128 VR Pin Reference	RAGE 128 VR Signal Name	RAGE XL Signal Name
A9	Memory Data / MPP2 Data / LCD Interface Data	LPVSS
B4	Memory Data / MPP2 Data / LCD Interface Data	TX2P
B5	Memory Data / MPP2 Data / LCD Interface Data	TX1P
B6	Memory Data / MPP2 address strobe / I2CCLK / LCD Interface Data	TX0P
B7	Memory Data / DVS2 data / LCD Interface Data	TXCP
B8	Memory Data / DVS2 data / LCD Interface Data	N/C
B9	Memory Data / Zoom Video Ctrl / LCD Interface Data	LPVDD
C4	Memory Data / MPP2 Data / LCD Interface Data	TXVSSR
C5	Memory Data / MPP2 data / LCD Interface Data	TXVDDR
C6	Memory Data / MPP2 Data Strobe / I2CDATA / LCD Interface Data	TXVSSR
C7	Memory Data / DVS2 data / LCD Interface Data	TXVDDR
C8	Memory Data / DVS2 data / LCD Interface Data	N/C
C9	Memory Data / Zoom video ctlr / LCD Interface Data	N/C
D2	LCD Interface Clock	N/C
D5	Memory Data / MPP2 data / LCD i/f data	N/C
D6	Memory Data / DVS2 data / LCD i/f data	N/C
E4	LCD i/f Display enable	MONDET
M18	Data Strobe (upper 32 bits DDR)	DFPCLK
M19	Memory Clock bar (upper 32 bits DDR)	N/C
M20	Memory Clock (upper 32 bits DDR)	N/C
N18	Data Strobe (lower 32 bits DDR)	CKE
N19	Memory Clock bar	N/C
R3	RBF#	N/C
U13	Future AGP4x support	N/C
U16	M66EN	PCI33EN
U17	CS3 Bank 3 chip select	N/C
U19	Memory Address line	MA10
U20	Select Bank	MA11
U4	Future AGP4x support/AGP/PCI power management output signal	N/C
U5	Future AGP4x support	N/C

Table 3-23 Pinout Differences: RAGE XL vs. RAGE 128 VR (Continued)

RAGE XL and RAGE 128 VR Pin Reference	RAGE 128 VR Signal Name	RAGE XL Signal Name
V4	Future AGP4x support/Power management input from AGP bus	N/C
V17	CS2 Bank 2 chip select	DFPDAT

Note: N/C means not connected.

3.11.3 Function Support Differences between RAGE XL and RAGE PRO

Table 3-24 Function Support Differences: RAGE XL vs. RAGE PRO

Function	RAGE PRO	RAGE XL
32-bit memory interface	No	Added 32-bit memory interface to support SDRAM
3D Enhancements required by PC98	None	• Bilinear Interpolation of Texture Alpha (eliminates blocky clouds, explosions and exhaust) • Modulate Alpha Function (Texture Alpha * Interpolated Alpha) • Composite Alpha Modulate (Primary Texture Color * Secondary Texture Alpha) • Fog Table Integration • Extra Alpha Blend Weight Choices: iALPHA_BLND_SRC and iALPHA_BLND_DST • Properly handle 1x1 and 2x2 texture maps in bilinear interpolation mode • CI8 - support [RGB555, RGB565, RGB888, ARGB8888] modes
Chip Select	Supports up to four Memory banks with CS2 and CS3 multiplexed onto MA10 and MA11.	Supports only up to two memory banks. There are no CS2, and CS3 pins. MA10 and MA11 are dedicated address pins.
DVD Subpicture	No	Yes. This feature is identical to that in RAGE 128.
EDO Memory Support	Yes	No
External DAC	Yes	No
Full Power Management	Only D0 and D3	All states (D0, D1, D2, and D3).

Table 3-24 Function Support Differences: RAGE XL vs. RAGE PRO

Function	RAGE PRO	RAGE XL
Alpha Blending	No	Supports video and graphics alpha blending ARGB8888.
GUI Command FIFO Size	192 entries	512 entries.
Host Bus Interface	Dedicated IDSEL pin in PCI-33	IDSEL in on pin SBA[7].
Nand Tree Implementation	No	Yes
Power	Pure 3.3V device.	Mixed 3.3V, 2.5V device.
Straps	Straps are on MD bus.	Straps are on MA Bus.
TMDS Panel Interface	No	Supports Panel interface including BLON (MONID0), DIGON (MONID3), MONDET, DFPCLK and DFPDAT.
VFC Interface	Yes	No

3.11.4 Power Differences between RAGE XL and RAGE PRO

Table 3-25 Power Differences: RAGE XL vs. RAGE PRO

Pin	RAGE PRO	RAGE XL
AVDD/PVDD	3.3V	2.5V
VDDC	3.3V	2.5V
VDDR	3.3V	3.3V
VREF*	Only supports LVTTL standard. VREF should be left open.	Supports only LVTTL standard. VREF is either connected to 3.3V or left open.

* Note: The VREF was originally designed to support DDR memory. It had its own power rail which was only used by DDR differential receivers. However, this DDR support (based on RAGE 128) was not needed for Rage XL. Thus, VREF's pad was then modified to tap into the ring power rail (VDDR) as part of the overall power improvement in Rage XL. It can be either connected to 3.3V or left it open. In either cases, Rage XL functionality is not affected.

3.11.5 Similarity and Differences between RAGE XL and RAGE Mobility

RAGE XL and RAGE Mobility are based on the same source code. The same custom macros for dual port DRAMs, PLLs and DACs are used in both chips. As a result, the electrical and timing characteristics of these two chips are very similar. The following table lists similarities and differences between these two chips.

Table 3-26 Feature Comparison: RAGE XL vs. RAGE Mobility

Feature	RAGE Mobility	RAGE XL
Integrated TV Out	Yes	No
Dual CRTC and DAC	Yes	No
Second HW Cursor / HW Icon	Yes	No
Integrated TMDS transmitters	No	Yes
Integrated LVDS transmitters	Yes	No
Full Power Management	Yes	Yes
Panel Control	Yes	No
Spread Spectrum	Yes	No
ZVPORT	Yes	No (XL has ITU-601 in rev B41 only)
LT GPIO	Yes	Yes (mapped to GPIO[17:14] for MONID[3:0]

Chapter 4
Functional and Interfacing Descriptions

The RAGE XL controller comprises several major subsystems and interfaces as shown in the figure below. This chapter briefly describes its functionality.

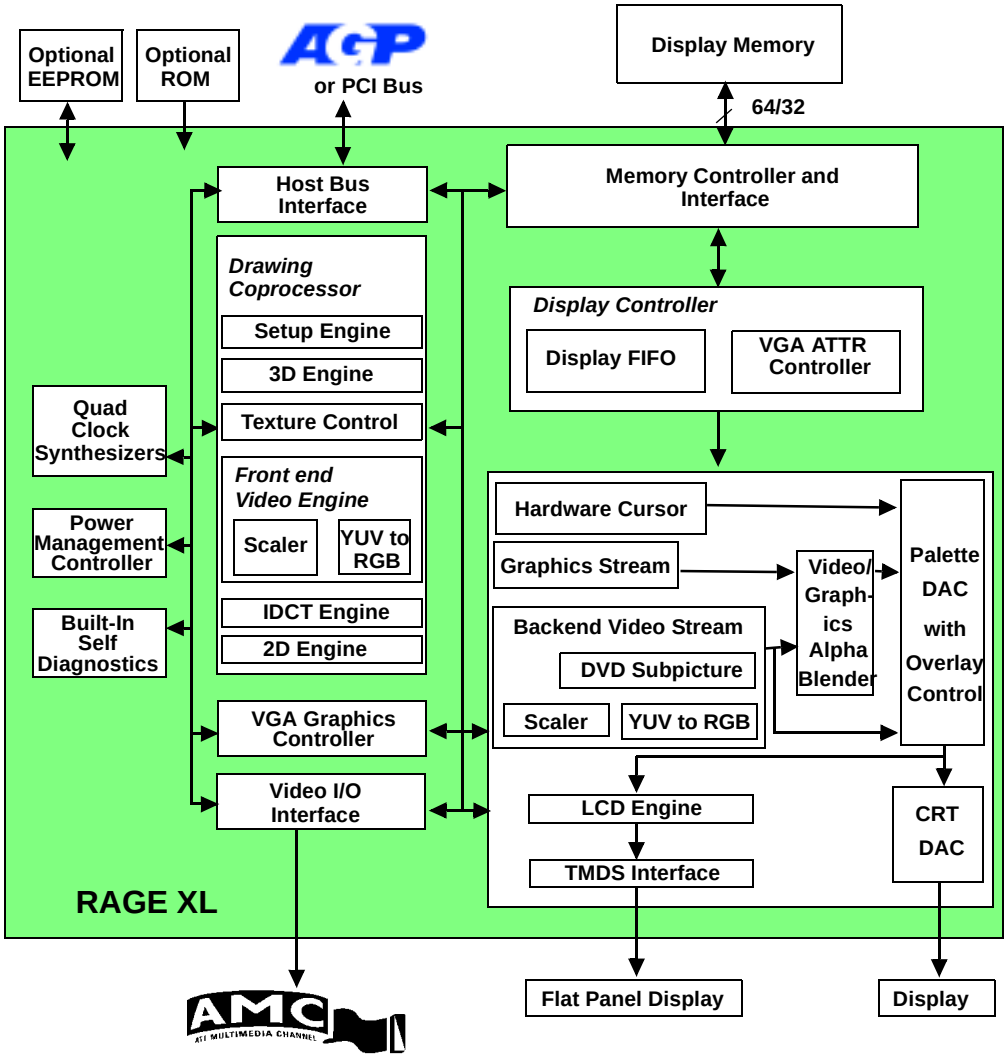


Figure 4-1. RAGE XL Functional Block Diagram

4.1 3D Graphics Coprocessor

The 3D graphics coprocessor offers a number of orthogonal pixel processing features associated with the rendering of 3D images. These coprocessor functions were chosen to accelerate the features of both Microsoft's D3D and Apple's QuickDraw 3D RAVE interfaces. Drivers will be available for all major operating systems and API.

RAGE XL includes a triangle setup engine. This engine needs only color, alpha, Z, U and V information at vertices of triangles to successfully draw Gouraud shaded or perspectively correct texture mapped triangles. The setup engine significantly reduces the CPUs load in 3D graphics applications, giving applications more CPU time to perform non-setup related tasks.

Pixels to be displayed can be further modified by alpha blending with pixels in the destination, by fogging pixels with a fog color, and in the case of texture mapping, by lighting them. Depth buffering is achieved by associating a 16-bit Z value with each pixel. The Z, Alpha, and fog color for each new pixel is supplied from interpolators within the 3D coprocessor. In case of texture mapping, the Alpha factor may even be stored in the texture map on a pixel-by-pixel basis.

Pixels in the 3D coprocessor are always operated on as 24-bit entities (8 bits each of Red, Green, and Blue). Other pixel sizes, i.e., 8-bit and 16-bit, are dithered by the 3D graphics subsystem to output at the desired pixel size.

The 3D coprocessor contains a powerful texture mapping engine. This engine takes a series of precomputed maps (mip maps) and selects texels from these maps in a way that allows them to look perspectively correct. Texels can be filtered in a number of ways, and then lit (lightened or darkened). Once the texel is formed by filtering and lighting, any of the pixel processing modes mentioned previously can be applied to the texel.

The 4K texture cache greatly reduces the memory bandwidth needed to support texture mapping.

With AGP support, texture maps can be stored in system memory and pulled into the local texture cache as needed. This rids the system of the need to add significant amount of local frame buffer memory in order to support multiple detailed texture maps, and allows applications to support a richer and more realistic environment.

4.2 2D Engine

This is a fixed-function unit that runs concurrently with the host processor. It is dedicated for drawing operations that include rectangle fill, line draw, polygon boundary lines, and polygon fill. A sophisticated pixel data path allows monochrome-to-two-color expansion, solid color fill, screen-to-screen bitblts, fixed pattern fill, general pattern fill, general patterns with rotation, and host-to-screen data transfers. Flexible bitblt trajectories allow hyper-efficient off-screen memory management, effectively increasing bitmap and font cache sizes and improving performance.

Other features include quick setup GUI engine that off-loads draw engine setup from the host CPU. A 16-function ALU and a 4-function source/destination color comparator allow for the combinations of source and destination in a multitude of ways, useful for operations such as image overlaying or transparent blits. Bit masking and scissoring can protect memory regions from being written.

All internal draw engine data paths are 64-bit wide. Full drawing features are available in 8, 15, 16, 24, and 32 bits-per-pixel (bpp) modes.

All draw engine registers are 32-bit wide. A 512x32 command FIFO improves throughput over the expansion bus. The additional 128 entries are dedicated to busmastering of 16x64 source and destination FIFO improving memory bandwidth throughput.

4.3 IDCT Engine

RAGE XL integrates an iDCT (Inverse Discrete Cosine Transform) engine along with motion compensation support for the acceleration of MPEG decoding. The acceleration hardware is fed directly from an advanced packet parsing engine, enabling high processing rates with minimal software overhead.

Using the advanced packet parsing engine also increases the parallelism between the hardware and software which ensures that the most is made of the host processor's power. This combination of hardware acceleration decreases the loading on the host processor to significantly below that of past MC-only engines, and enables quality software DVD playback on processors which, until now, had relied on dedicated hardware decoders. It can also provide acceleration for decode of HD0 level bitstreams.

The iDCT engine implements an IEEE 1180 compliant iDCT algorithm which, when combined with a run/level and dezig-zag formatter, off-loads a significant portion of the MPEG decoding process from the host processor. Run/level codes are combined with control words by the host processor in a packetized format, which the advanced packet parsing engine bus masters down from system memory over the AGP bus. The run/level codes are expanded and then dezig-zagged before being fed into the iDCT engine. Dezig-zagging is selectable through the register interface. There is also selection for intra/non-intra block support. The iDCT engine takes the dezig-zagged coefficients and performs a 2-D iDCT before buffering the result and sending it to the MC hardware.

The MC hardware allows for implementation of all motion compensation modes required for MPEG-2 support. It fetches data from the frame buffer based on control information supplied by the advanced packet parsing engine on a macroblock basis, combines the data from the frame buffer with the output of the iDCT engine through a full 9-bit signed adder, and then writes the result back to the frame buffer.

4.4 Display System

The display system comprises a number of subsystems as described below.

4.4.1 Extended VGA Graphics Controller

The VGA portion of the graphics controller is fully register compatible with the VGA standard and is BIOS-compatible with VESA super VGA drivers.

4.4.2 CRT Controller (CRTC)

The CRTC subsystem supports such standard features as overscan, video memory sizes up to 8MB, and screen resolutions up to 1920x1080 non-interlaced.

4.4.3 Display Controller

The display controller subsystem consists of three units as follows:

- Display FIFO to manage the memory interface for displayed pixel data.
- Enhanced attribute controller for VGA.
- 24-bit palette.

The display controller supports VGA graphics modes up to 1600x1200 (85 Hz), VGA text modes up to 132 columns, and accelerator display modes up to 1600x1200 (85 Hz) and 1920x1080 (72 Hz).

4.4.4 Hardware Cursor

The hardware cursor logic supports a 64x64x2 memory-mapped cursor that is also XGA function compatible. The hardware cursor may be used in any display mode supported by this controller. It has three modes: transparent, complement, and two solid colors.

4.4.5 Video Coprocessor

The video coprocessor has an optimized data path designed for scaling, filtering, and color space conversion. An integrated dual 768-pixel line buffer provides superior vertical scaling and interpolation. Graphics and video keying capabilities and a window controller allow for overlaying of the graphics and video data streams. This enables simultaneous display of 24-bpp video and 8/16/24/32-bpp graphics.

4.4.6 DVD Subpicture

RAGE XL includes a DVD subpicture decoder and scaler with the following features:

- Subpicture Decoder:
  - Operates on 2 bpp and produces YUV444 and K.
  - Compliant to DVD specifications.
  - Button support.
  - Maximum source width: 720 pixels
- Subpicture Scaler:
  - Operates on YUV444 and K from the subpicture decoder.
  - 2-tap vertical up/down scaling.
  - 2-tap horizontal up/down scaling.
  - Subpicture can be shifted anywhere within the overlay window.
  - Allows pixel replication or blending.
  - Supports “bob and weave”.

4.4.7 Palette and CRT DAC

The internal palette and CRT DAC subsystem consists of a triple 256x8 SRAM palette and a triple 8-bit DAC. It supports the following features:

- Pixel clock rates up to 230 MHz for resolutions up to 1920x1080 (72 Hz).
- Refresh rates up to 200 Hz.
- Built-in DAC reference generation.
- Monitor detection.
- Direct 24-bit color.
- Separate or composite horizontal and vertical sync signals.
- Optimized slew rate control for the RGB analog output for low EMI emission.

Note: The CRT DAC is used by the display controller that is actively selected for the CRT or monitor.

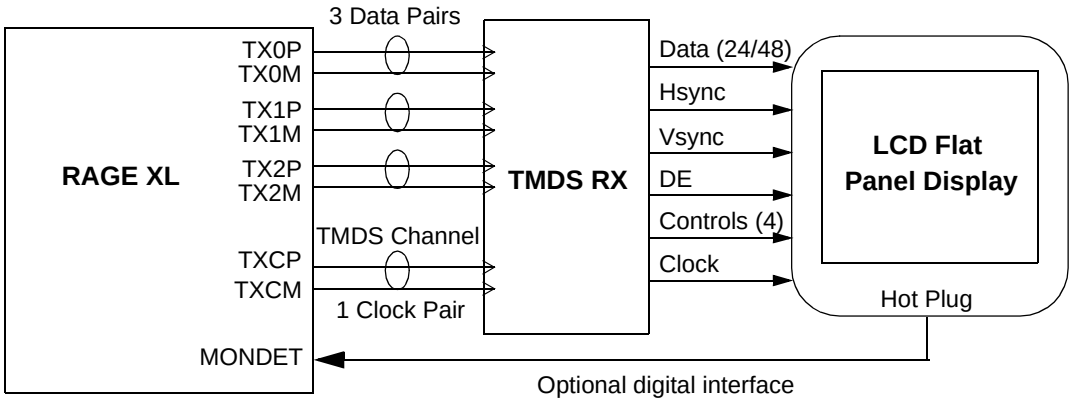
4.4.8 LCD Engine and Panel Interface

RAGE XL has a built-in interface for a range of LCD panels, including TFT, with different color depth and pixel packing formats.

The LCD engine processes the RGB (digital) signals from the palette DAC, then sends the output to the LCD panel for display through a built-in TMDS transmitter. This block features frame modulation and dithering, on the TFT panel, to generate grey levels.

4.4.9 TMDS Interface

The TMDS transmitter is implemented to reduce EMI and narrow the interface to the panel. The figure below shows data flow from RAGE XL to a single pixel TFT panel.



Note: TMDS channel includes output pins TXCP, TXCM, TX0P, TX1P, TX1M, TX2P, TX2M

Figure 4-2. RAGE XL TMDS Interface

4.4.10 Ratiometric Expansion

The Ratiometric Expansion logic controls the process that scales up the active display area of the current graphics mode by filtering pixels (2-tap filter in the horizontal direction) and lines (2-tap filter in the vertical direction). Whenever the resolution of the current graphics mode is smaller than that of the LCD panel, this block is used to generate the frame that fills the entire LCD panel. Ratiometric expansion uses replication or blending to support the graphics and text modes.

4.5 Chip Power Management

The RAGE XL sub-micron CMOS integrated circuit is optimized for low power consumption during normal operation. It provides mixed 3.3V and 2.5V operation through dedicated power pins for internal (core) logic, host bus, memory and display interface. The internal logic always operates at 2.5V to minimize power consumption. A flexible clock synthesizer is used to generate independent memory, 2D/3D and video clocks.

The Advanced Chip Power Management logic supports four device power states — On, Standby, Suspend and Off — defined for the OnNow Architecture. Each power state can be achieved by software control bits. By implementing Power Management Capability registers in PCI configuration space, the chip becomes directly controllable from system BIOS.

Clocks to every major functional block (2D, 3D, video, LCD out, display pipe, video scaler and subpicture) are controlled by a unique dynamic clock switching technique that is completely transparent to the software. By turning off the clock to the block that is idle or not used at that point, the power consumption is significantly reduced during normal operation. If the clock is needed, it can be restored within one clock without affecting overall performance of the chip.

4.6 Quadruple Clock Synthesizer

The internal clock synthesizer consists of four independent phase locked loops (PLL) capable of synthesizing any frequency up to 230 MHz. All PLLs have been optimized for low jitter graphics applications.

- The first PLL generates clocks for the CRTC, display controller, and palette DAC. This PLL can be reprogrammed by the BIOS for each display mode.
- The second PLL generates the clock for the drawing coprocessor.
- The third PLL is used to generate the 66 MHz and 133 MHz internal clock synchronous AGP bus operations.
- The fourth PLL generates the clock for the memory controller.

4.7 ATI Multimedia Channel (AMC)

The AMC represents a collection of hardware and software components designed to facilitate the use of ATI products for multimedia applications. It consists of a non-chip audio bus, and three ports into the graphics controller. The DVS port for video input into the graphics controller, the MPP port for video input and output from the graphics controller, and the I^2C port for controlling attached devices.

The Multimedia Peripheral Port (MPP) Mode supported by AMC allows interface with external I/O devices. For example, compressed data can be transferred by means of MPP from the host (CPU) to the MPEG-2 decoder for DVD applications.

The Digital Video Stream (DVS) port accepts industry standard video formats, and allows easy attachment of video decoders and hardware MPEG-2 decoders. The DVS port provides for decoded video data to stream back to the graphics controller.

The I^2C is an industry standard serial bus that allows control and programming of a wide range of peripherals. RAGE XL incorporates an I^2C interface to allow programming of peripherals such as video decoders, TV tuners, teletext decoders, and volume control.

4.8 Host Bus Interface

RAGE XL supports the Accelerated Graphics Port (both AGP 66 MHz and 133 MHz). Addressing modes include sideband address support. AGP enabled controllers can access directly large texture maps stored in the system memory. Applications that make use of large numbers of 3D objects can reduce the amount of memory required in the frame buffer.

In PCI configuration, RAGE XL acts as a target device, supporting 32-bit memory and I/O operations and byte lane swapping. With full 32-bit address decoding available in PCI, it can map the Direct Memory Interface to 4GB of memory space on a 16MB boundary.

The controller achieves zero wait-state memory read/write burst cycles with burst access. It also supports Block I/O decoding.

Bus mastering allows data transfer operations without CPU intervention. In bus master mode, the controller will take control of the PCI bus by driving the address and control signals.

Bus mastering functions between (1) system memory and frame buffer, (2) system memory and MPP, and (3) system memory and GUI engine, allow all data transfer operations to be off-loaded from the host processor onto the motherboard chip set.

AGP Bus Configuration is shown in *Figure 4-3.*

PCI Bus Configuration is shown in *Figure 4-4.*

4.8.1 AGP Bus Interface

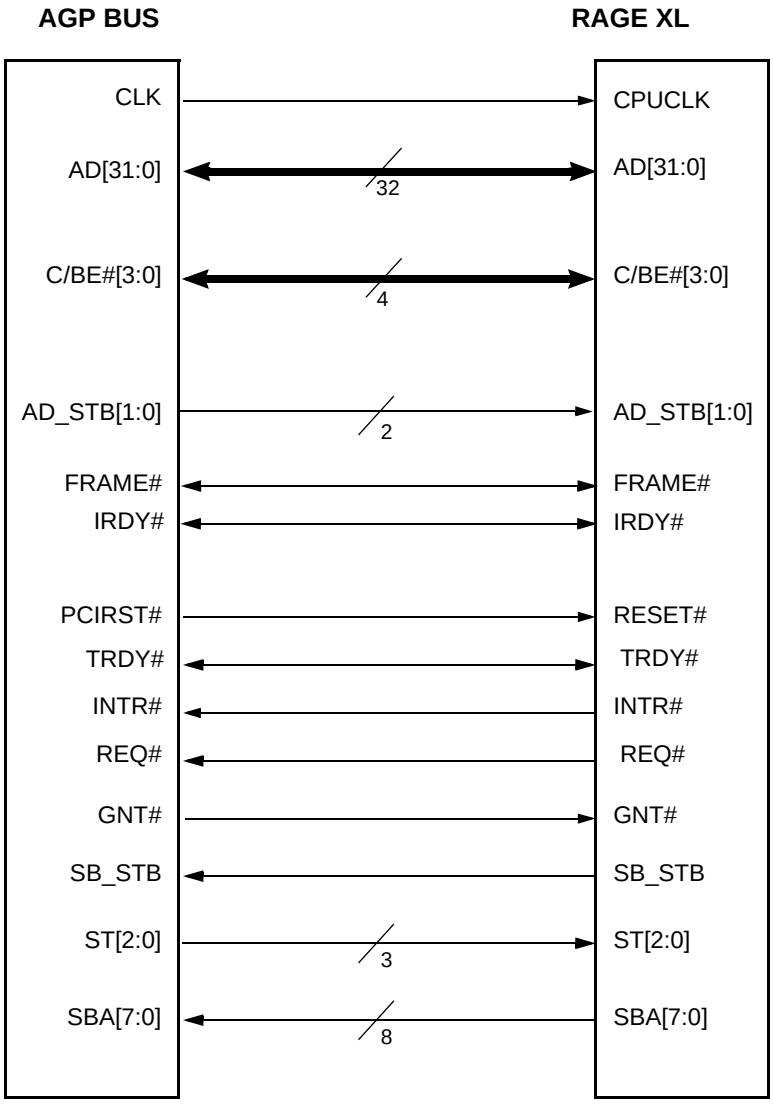


Figure 4-3. AGP Bus Configuration

4.8.2 PCI Bus Interface

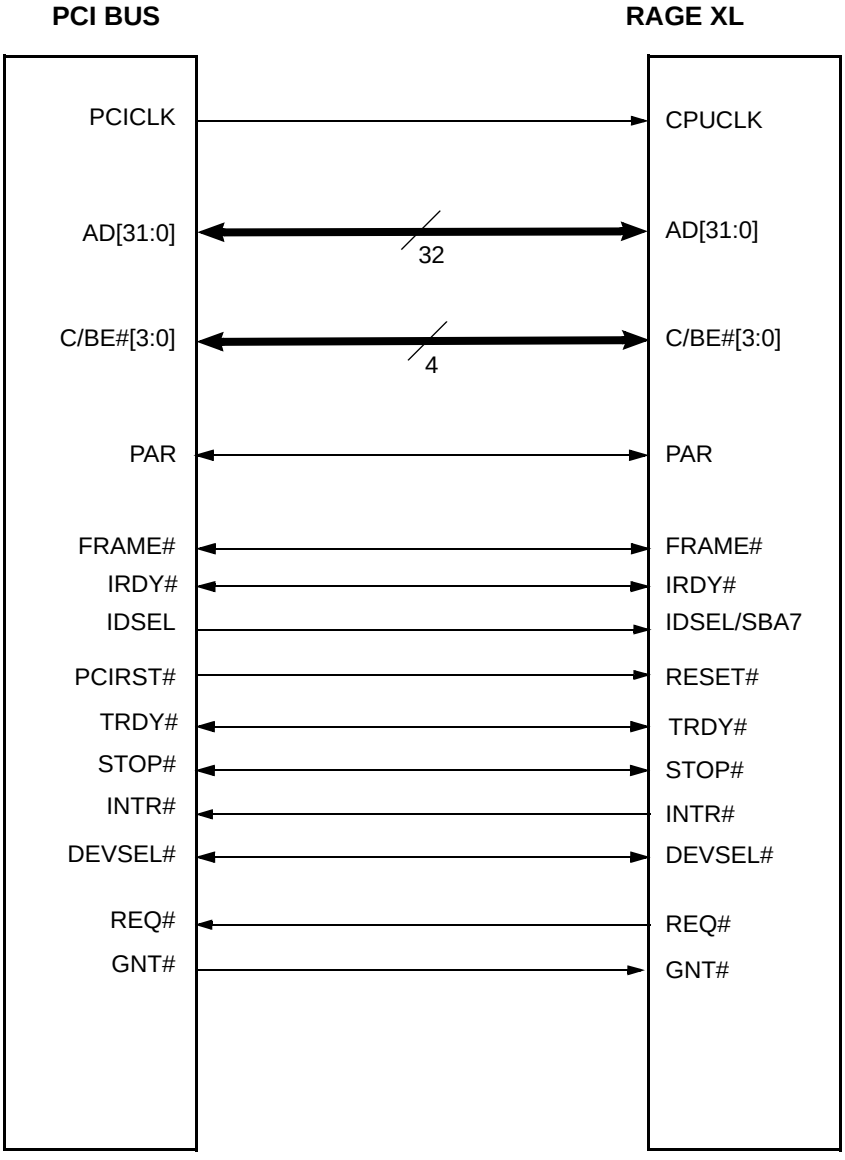


Figure 4-4. PCI Bus Configuration

4.9 Memory Controller and Interface

The memory controller subsystem arbitrates requests from the direct memory interface, the VGA graphics controller, the drawing coprocessor, the display controller, the video scaler, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

The memory interface of this controller supports the following memory devices: **SDRAM** or **SGRAM** — 128Kx32x2, 256Kx32x2, 512Kx16x2, 512Kx32x2, and 512Kx32x4.

4.9.1 Memory Configurations

The following two tables show the number of memory devices that are needed to support various sizes of frame buffer.

Table 4-1 64-bit Wide Memory Configurations

Memory Type	Row x Col.	# of Devices / Frame Buffer		
		2MB	4MB	8MB
SGRAM 128Kx32x2 (8 Mbit)	10 x 8	2	4	-
SGRAM 256Kx32x2 (16 Mbit)	11 x 8	-	2	4
SGRAM 512Kx32x2 (32 Mbit)	12 x 8	-	-	2
SDRAM 512Kx16x2 (16 Mbit)	12 x 8	-	-	4

Table 4-2 32-bit Wide Memory Configurations

Memory Type	Row x Col.	# of Devices / Frame Buffer		
		2MB	4MB	8MB
SDRAM 512Kx16x2 (16 Mbit)	12 x 8	-	2	-
SDRAM 512Kx32x4 (64 Mbit)	13 x 8	-	-	1

Note: SGRAM block write is not supported in x32 mode.

4.9.2 Memory Interface Mapping

The table below is for 64-bit wide memory interface. For a 32-bit wide interface, the mapping is identical, with the following exceptions:

- Memory data uses MD[31:0] only.
- DQM[3:0] of the DQM bus are used.
- DSF is not used (since SGRAM block-write in 32-bit wide interface is not supported).

Table 4-3 Memory Mapping

Pin Name	Memory Type					
	SGRAM	SGRAM DIMM			SDRAM	
	128Kx32x2 8 Mb	128Kx32x2 8 Mb	256Kx32x2 16 Mb	512Kx32x2 32 Mb	512Kx16x2 16 Mb	512Kx32x4 64 Mb
CAS#	CAS[0]	CAS	CAS	CAS	CAS	CAS
CKE	CKE	CKE	CKE	CKE	CKE	CKE
CS0	RAS1	CS0	CS0	CS0	-	-
CS[1]	CAS[1]	CS1	CS1	CS1	-	-
DQM[7:0]	DQM[7:0]	DQM[7:0]	DQM[7:0]	DQM[7:0]	DQM[7:0]	DQM[7:0]
DSF	DSF	DSF	DSF	-	-	MA[12]
HCLK	HCLK	HCLK	HCLK	HCLK	HCLK	HCLK
MA[9:0]	MA[9:0]	MA[9:0]	MA[9:0]	MA[9:0]	MA[9:0]	MA[9:0]
MA10	-	-	MA10	MA10	MA10	MA10
MA11	-	-	-	MA11	MA11	MA11
MD[63:0]	MD[63:0]	MD[63:0]	MD[63:0]	MD[63:0]	MD[63:0]	MD[63:0]
RAS#	RAS[0]	RAS	RAS	RAS	RAS	RAS
WE#	WE#	WE#	WE#	WE#	WE#	WE#

SDRAM implementation for RAGE XL using 512Kx16x2 devices is shown in *Figure 4-5.*

An SGRAM implementation using 128x32x2 devices is shown in *Figure 4-6.*

An SGRAM implementation using 256x32x2 devices is shown in *Figure 4-7.*

An SGRAM implementation using 512Kx32x2 devices is shown in *Figure 4-8.*

An SDRAM implementation using a 512Kx32x4 device is shown in *Figure 4-9.*

An SO-DIMM Module Interface implementation is shown in *Figure 4-10.*

4.9.3 SDRAM Interface with 512Kx16x2 (16 Mbit) Devices (RAGE XL)

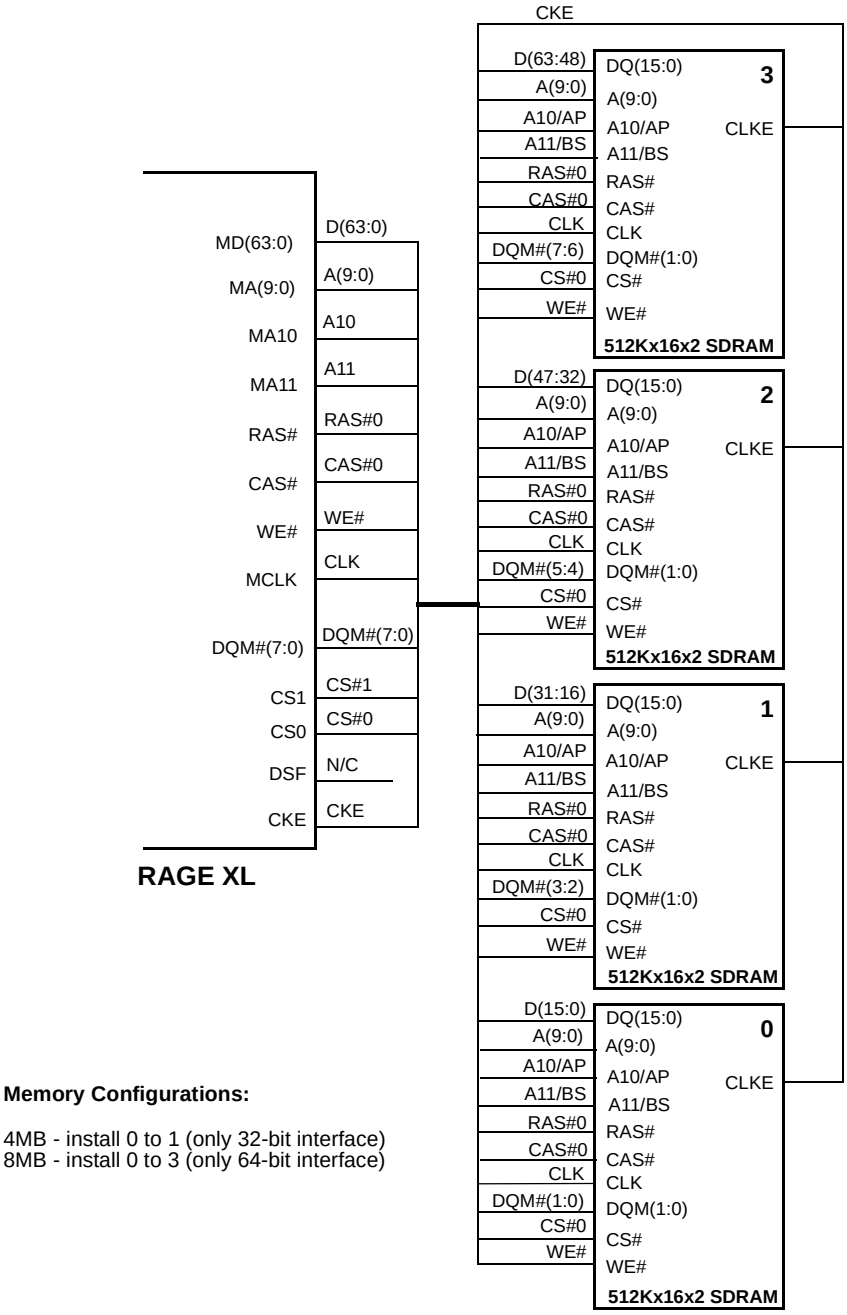


Figure 4-5. SDRAM Implementation (16 Mbit) - RAGE XL

4.9.4 SGRAM Interface with 128x32x2 (8 Mbit) Devices

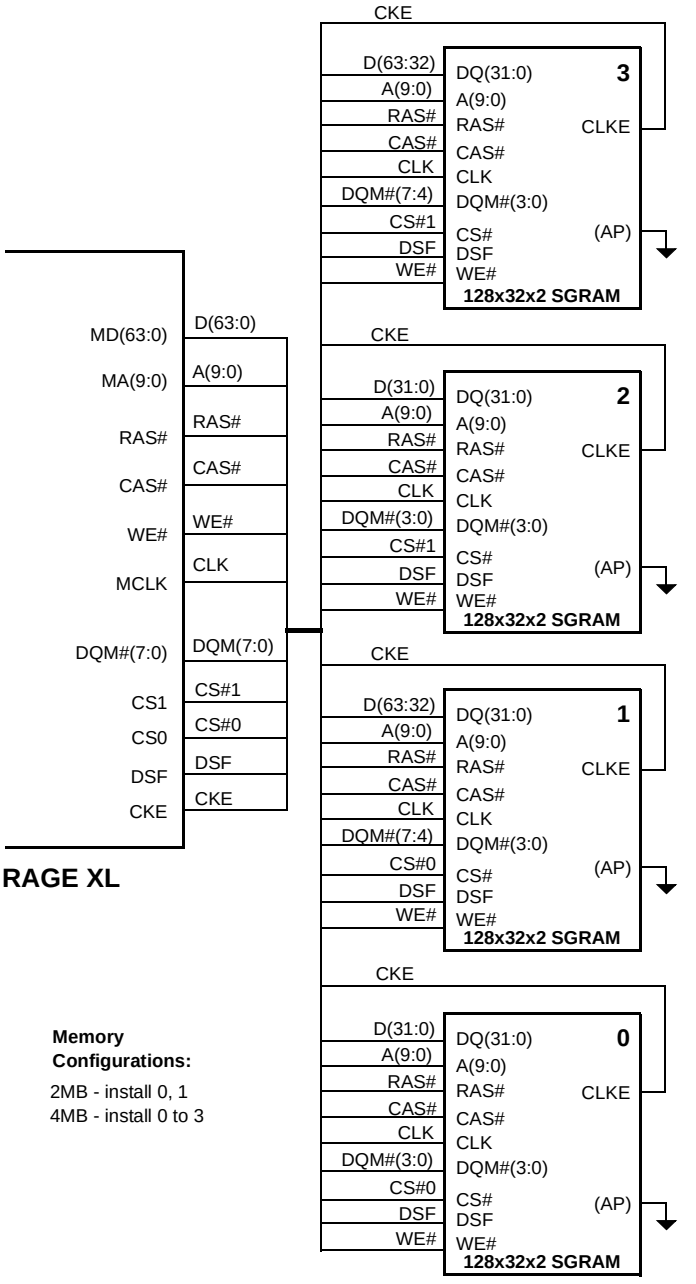


Figure 4-6. SGRAM Implementation (8 Mbit)

4.9.5 SGRAM Interface with 256x32x2 (16 Mbit) Devices

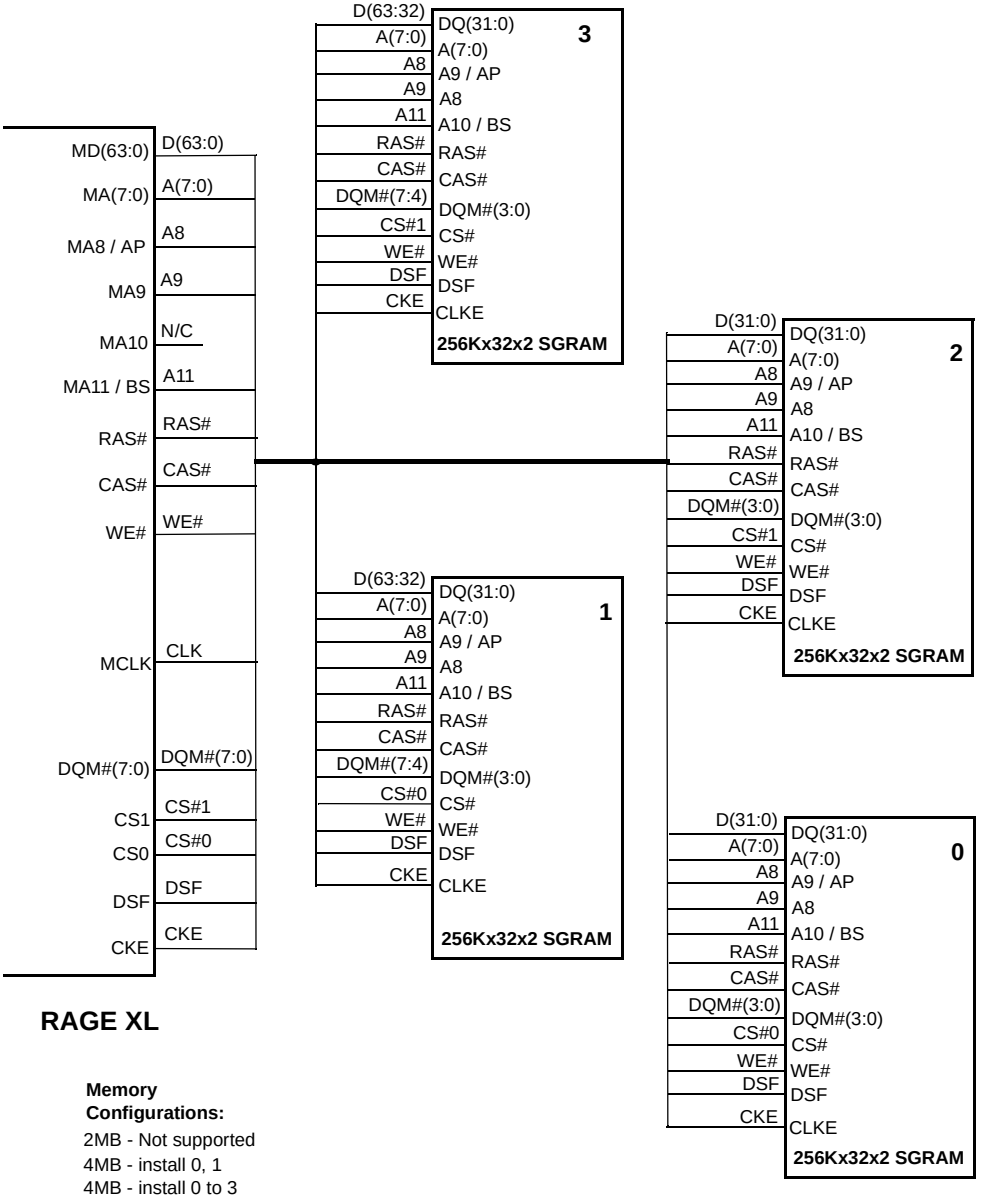


Figure 4-7. SGRAM Implementation (16 Mbit)

4.9.6 SGRAM Interface with 512Kx32x2 (32 Mbit) Devices

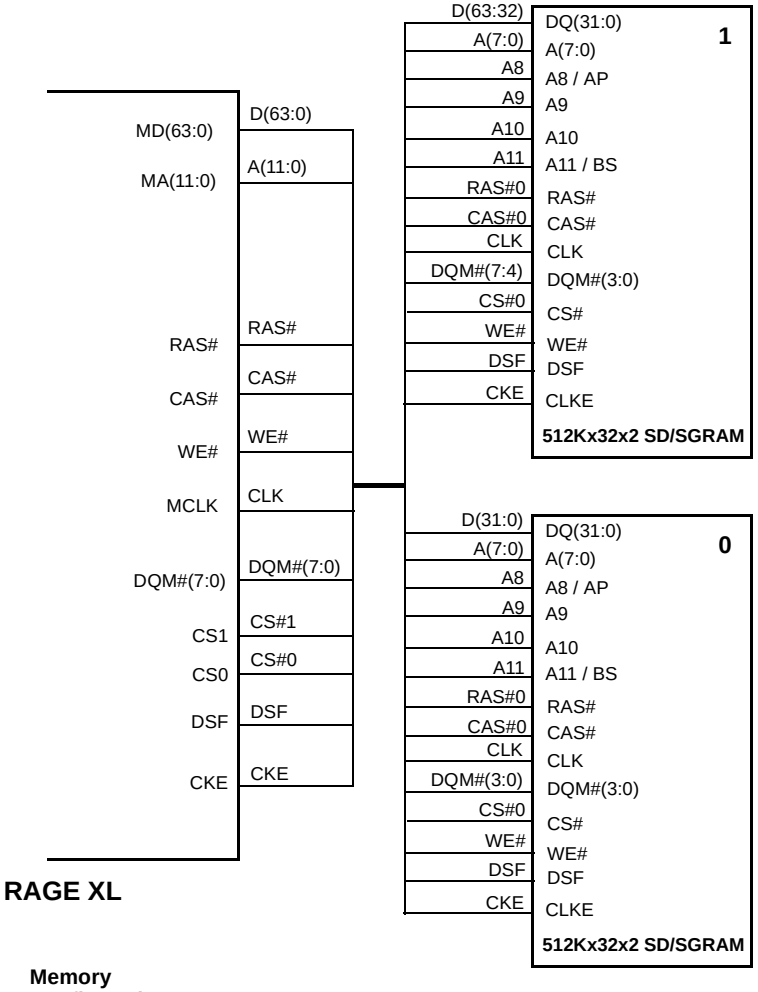


Figure 4-8. SGRAM Implementation (32 Mbit)

4.9.7 SDRAM Interface with 512Kx32x4 (64 Mbit) Devices

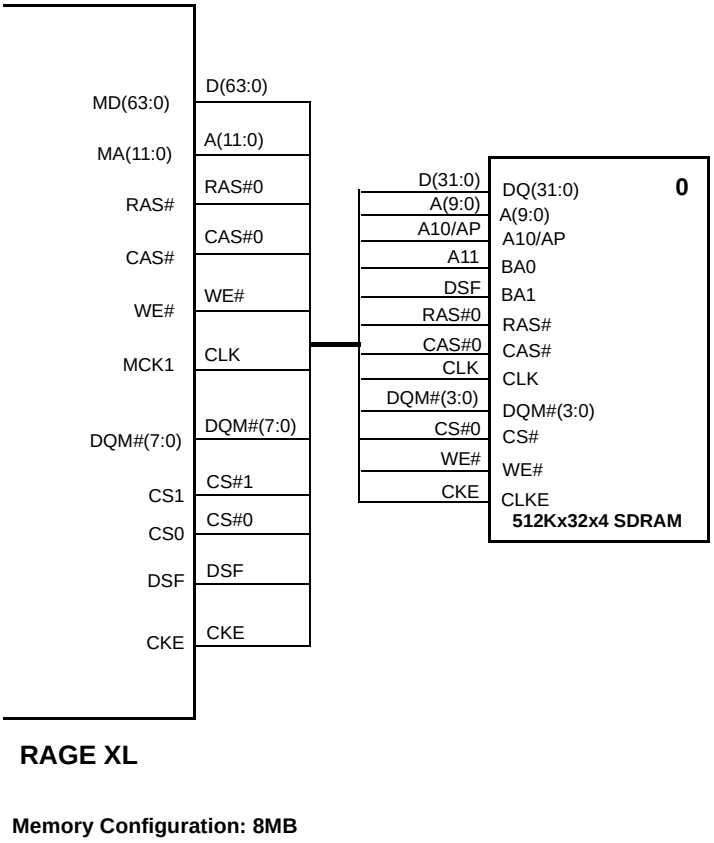


Figure 4-9. SDRAM Implementation (64Mbit)

4.9.8 SO-DIMM Module Interface

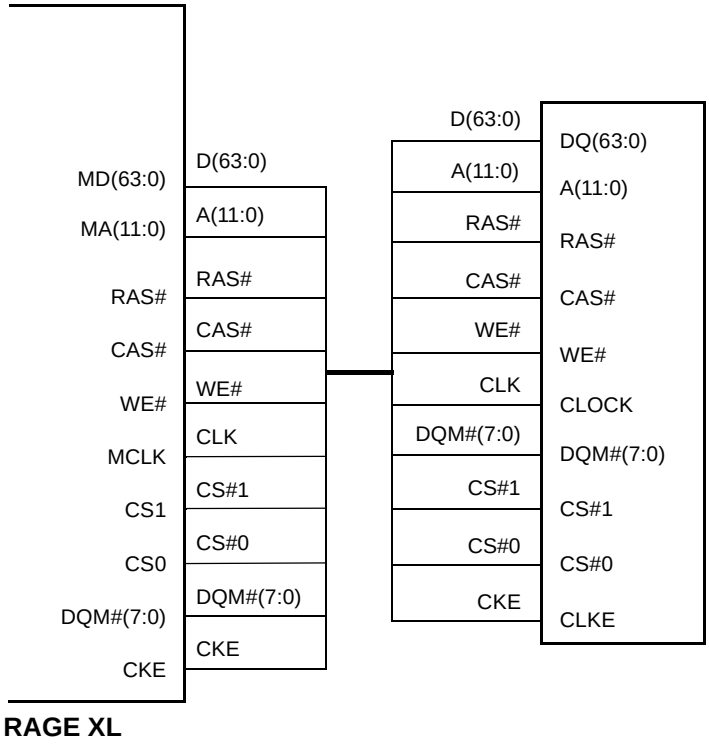


Figure 4-10. SO-DIMM Module Implementation

4.10 EPROM Interface

The video BIOS may be stored in either a 32K or a 64K EPROM (27256/27512), or integrated into the system BIOS. ATI offers a BIOS kit which is used for BIOS customization or integration of the video BIOS with the system BIOS (*see Figure 4-11.*). This kit allows certain BIOS options to be created, for example:

- 32K or 36K non-paged (linear) BIOS.
- 64K BIOS.
- 128K BIOS.

Refer to the *mach64 BIOS Kit (BIO-G01000)* manual for additional information on the differences and trade-offs of the various options.

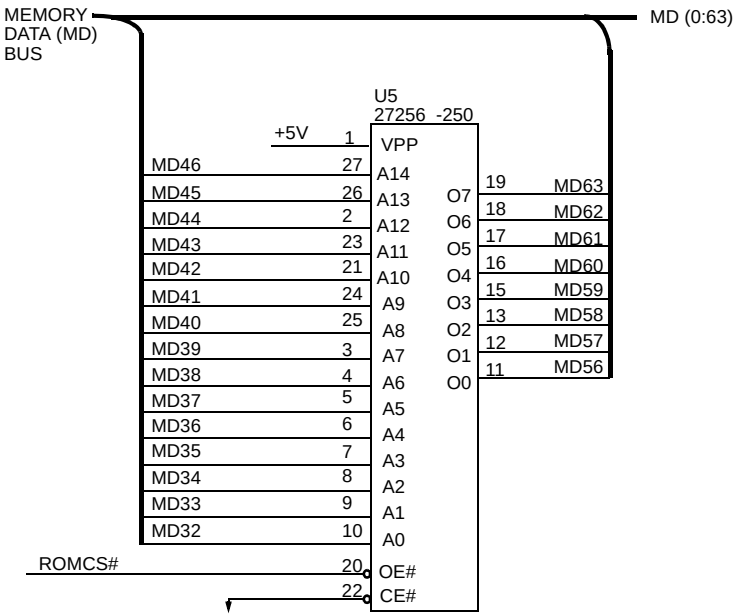


Figure 4-11. EPROM Interface

4.11 Flash Memory Interface

Up to 128K of flash memory is supported.

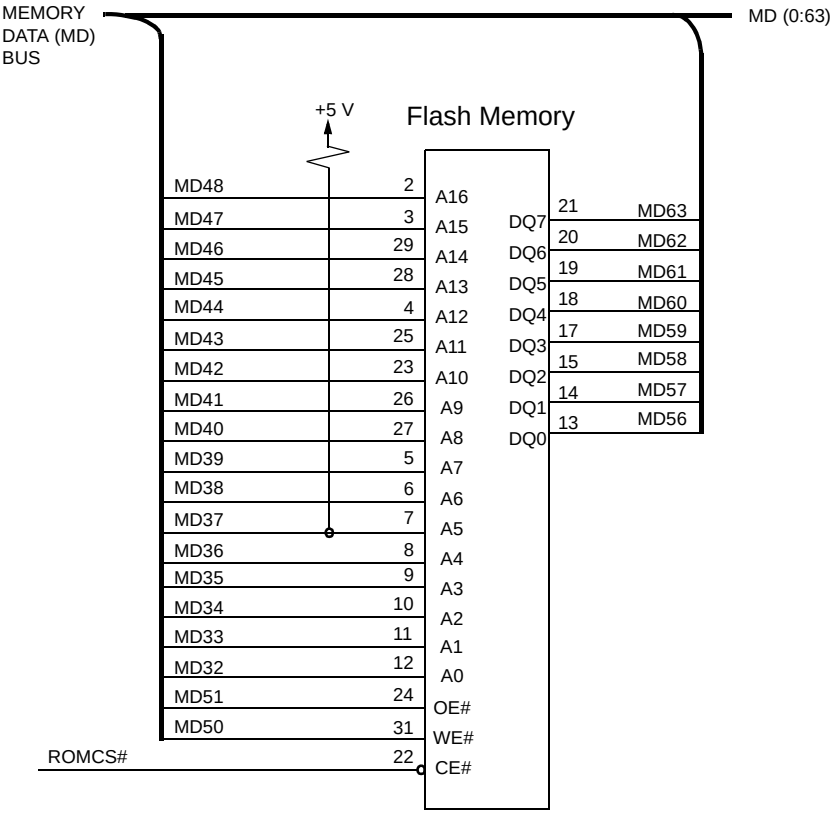


Figure 4-12. Flash Memory Interface

4.12 General Purpose I/O Control

Within RAGE XL there are 18 general purpose I/O pins. They are used to support the I^2C bus control, monitor ID and MPP port, and ATI Multimedia Channel (AMC) Interface.

4.13 ATI Multimedia Channel 2.0 Interface (AMC)

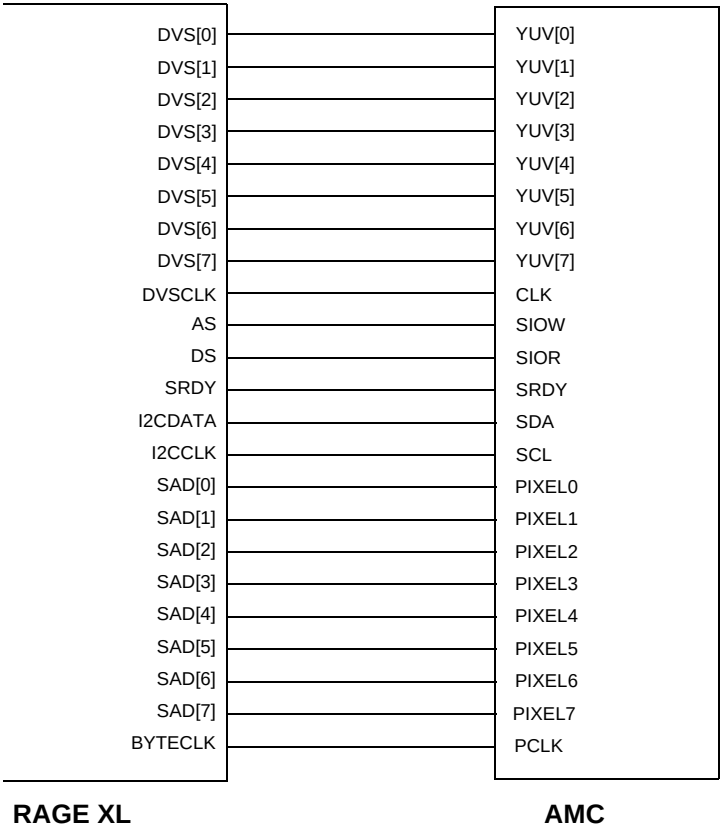


Figure 4-13. ATI Multimedia Channel 2.0 Interface

The AMC is a 40-pin connector that can operate in various modes under different conditions. The AMC pins have different functions under different modes.

4.13.1 DVS Mode

Digital Video Stream Mode supports a direct connection to a Brooktree Bt829, Bt827, Bt819, Bt817, or Bt815, Philips SAA7112 or SAA7111, Samsung KSO122, or ITT VPC32xx video decoder. *Figure 4-14* shows the 8-bit interface with the *RAGE XL* graphics controller.

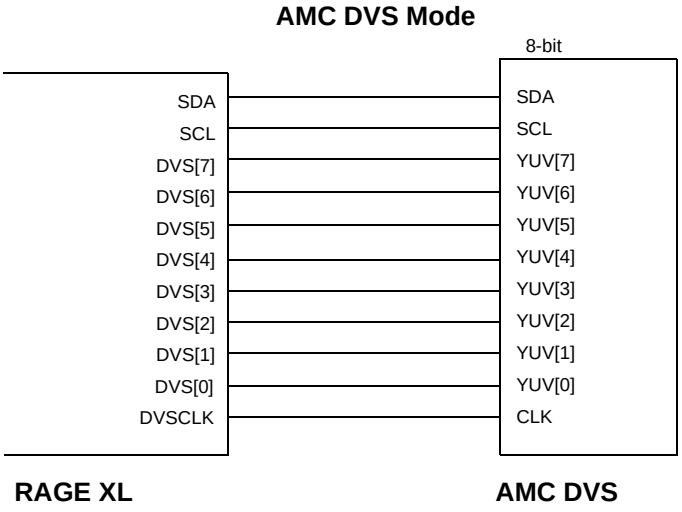


Figure 4-14. AMC DVS Mode (8 bit)

4.13.2 MPP Mode

Multimedia Peripheral Port Mode can stream data from the host memory out of this port. Timing and protocol can be programmed to support peripheral chips. By connecting this port to an external NTSC/PAL encoder, the display screen can be modulated to an NTSC/PAL TV signal. *Figure 4-15* shows the interface between external ImpacTV encoder and *RAGE XL* chip.

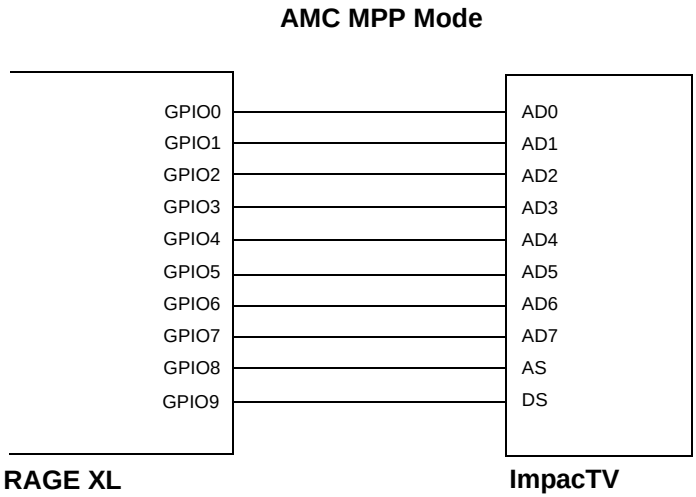


Figure 4-15. AMC MPP Mode

4.14 Analog Output Section

Each of the R, G, B lines on the board (see *Figure 4-16.*) is to be loaded with a 75Ω resistor. Diodes can be used to protect the controller from any large transient voltages which may enter from the connector when the monitor is connected.

Bypass capacitors can also be placed on all lines in order to filter the output. The RGB lines may also have inductors (ferrites) placed in series. This may be required in order to comply with FCC Class B requirements for radio frequency emissions. The proper value is determined as a trade-off between filtering the signals for FCC requirements and video signal clarity.

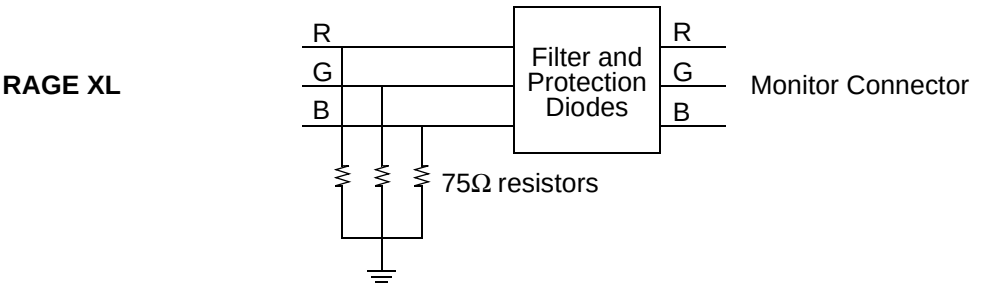


Figure 4-16. Analog Output

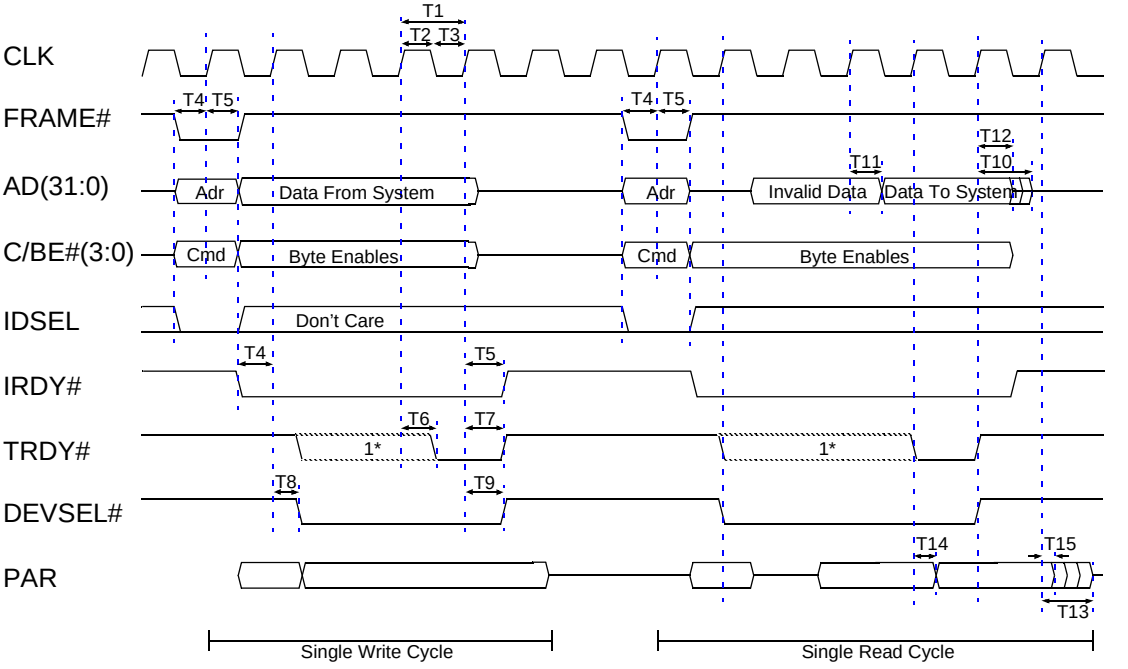
Chapter 5
Timing Specifications

5.1 Bus Timings

Timing specifications for PCI bus operations are given by:

- Single Read/Write Cycle Timing, see *Figure 5-1.*
- Disconnect On Burst Cycle Timing, see *Figure 5-2.*
- Burst Access Timing, see *Figure 5-3.*
- PCI Bus Master Operation Timing, *see Figure 5-4.*
- AGP AC Timing, see *Figure 5-6.* and *Figure 5-5.*
- Power Up and Reset Timing, see *Figure 5-7.*

5.1.1 Single Read/Write Cycle Timing



1* The minimum number of clocks from FRAME# active to TRDY# active is programmable.

Figure 5-1. Single Read/Write Cycle Timing - PCI Bus

5.1.2 Disconnect On Burst Cycle - PCI Bus

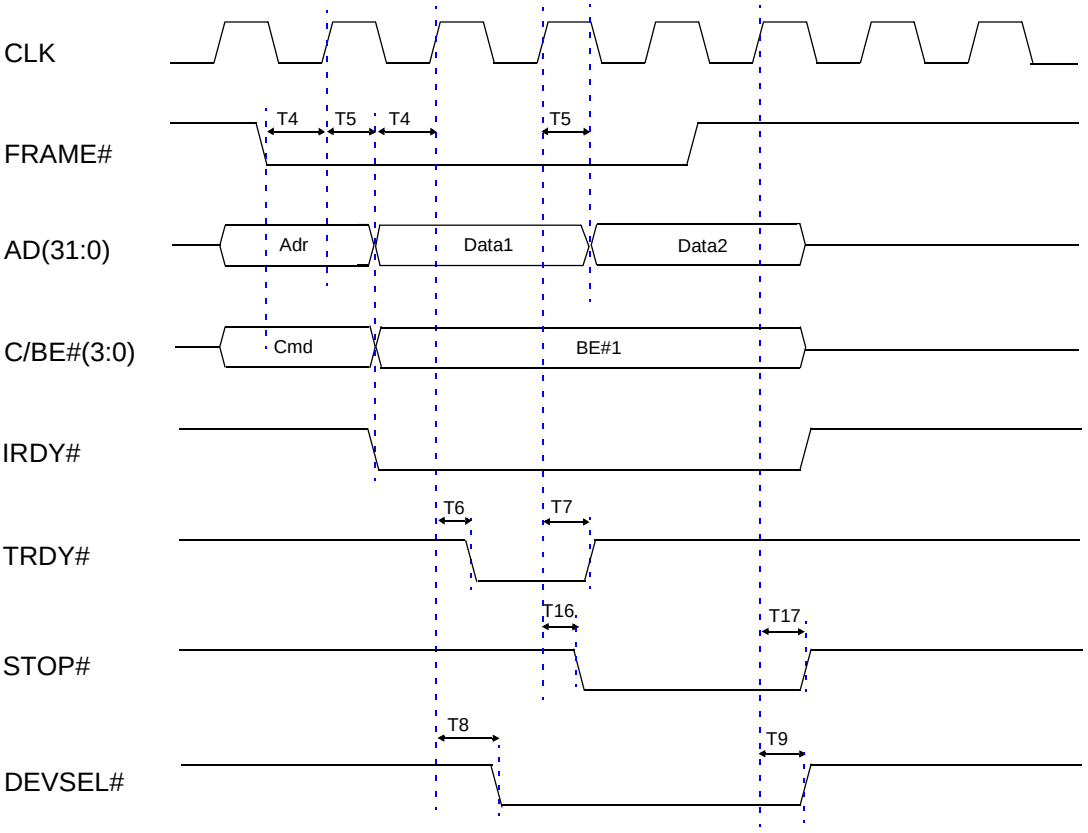


Figure 5-2. Disconnect On Burst Cycle - PCI Bus

5.1.3 Burst Access Timing - PCI

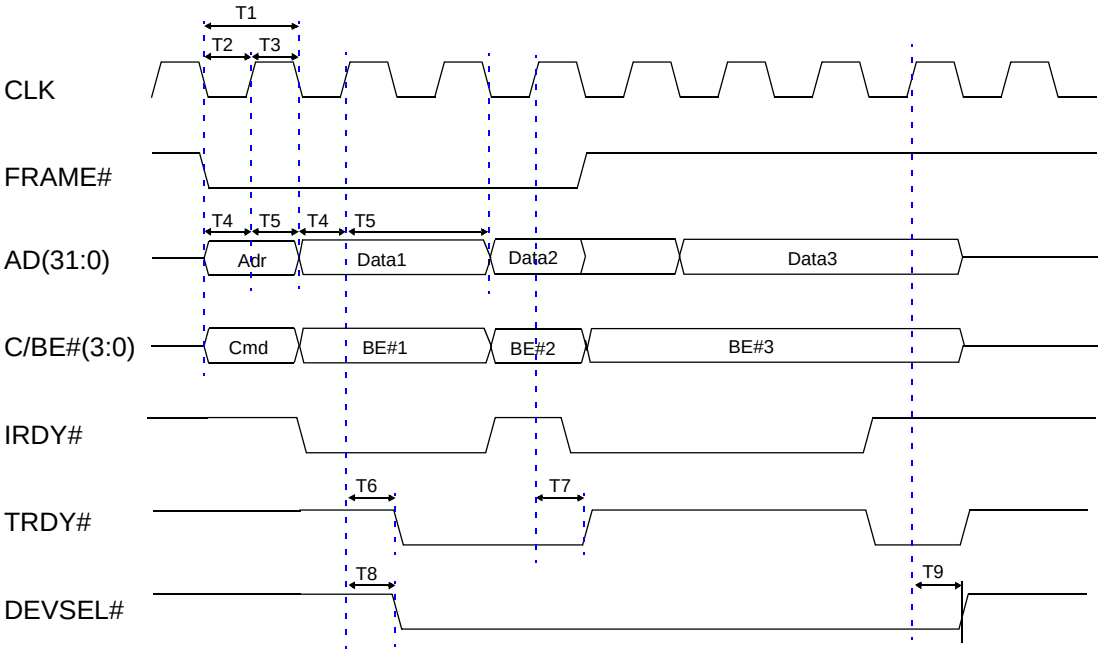


Figure 5-3. Burst Access Timing - PCI Bus

5.1.4 PCI Bus Master Operation

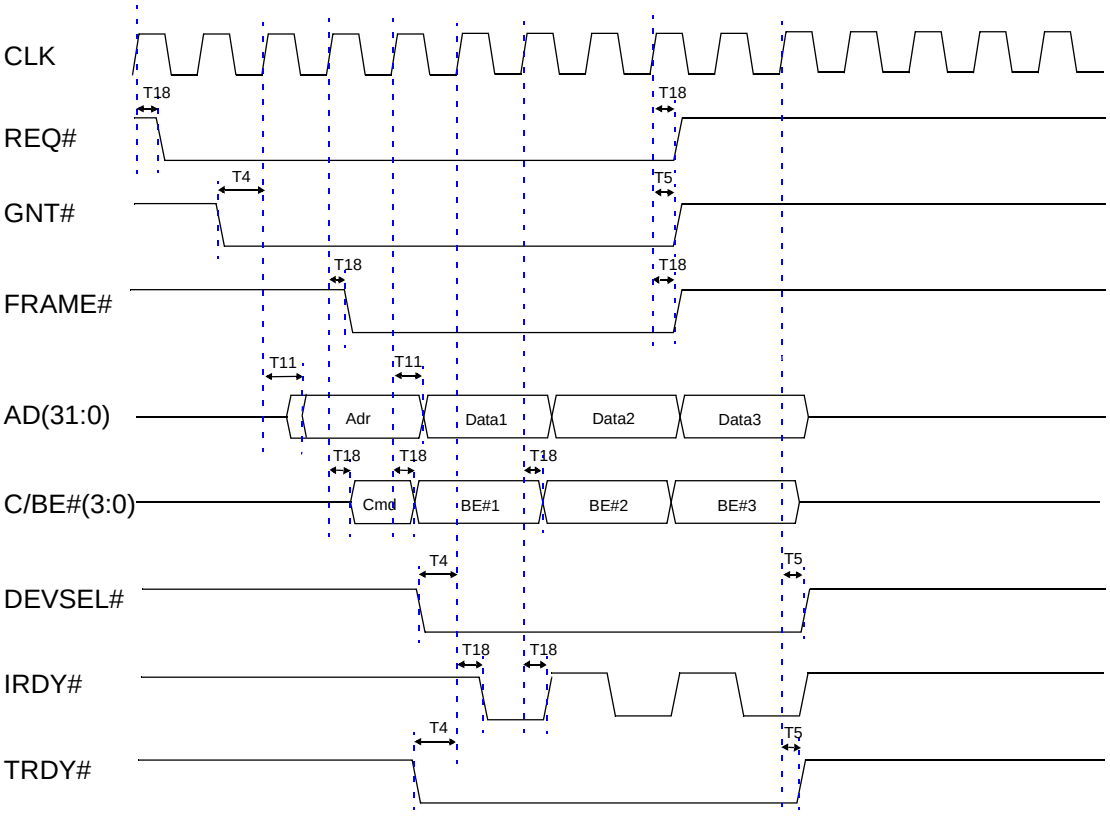


Figure 5-4. PCI Bus Master Operation

Table 5-1 PCI Bus Interface Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
T1	Bus Clock Period	30	-
T2	Bus Clock High Time	12	-
T3	Bus Clock Low Time	12	-
T4	Bus Input Signal Setup to CLK[a]	7	-
T5	Bus Input Signal Hold from CLK[a]	0	-

Table 5-1 PCI Bus Interface Timing Parameters (Continued)

Symbol	Description	Min.(ns)	Max.(ns)
T6	CLK to TRDY# active	2	11
T7	CLK to TRDY# inactive	2	11
T8	CLK to DEVSEL# active	2	11
T9	CLK to DEVSEL# inactive	2	11
T10	CLK to data output tri-state	2	20
T11	CLK to data output valid delay (data stepping buffer)	2	20
T12	CLK to data output invalid delay	2	-
T13	CLK to PAR tri-state	2	20
T14	CLK to PAR valid delay (data stepping buffer)	2	20
T15	CLK to PAR invalid delay	2	-
T16	CLK to STOP# active delay	2	11
T17	CLK to STOP# inactive delay	2	11
T18	CLK to signal valid delay	2	11

a. Bus input signals include FRAME#, AD(31-0), IDSEL, IRDY#, TRDY#, GNT#, DEVSEL#.

5.1.5 AGP Timing

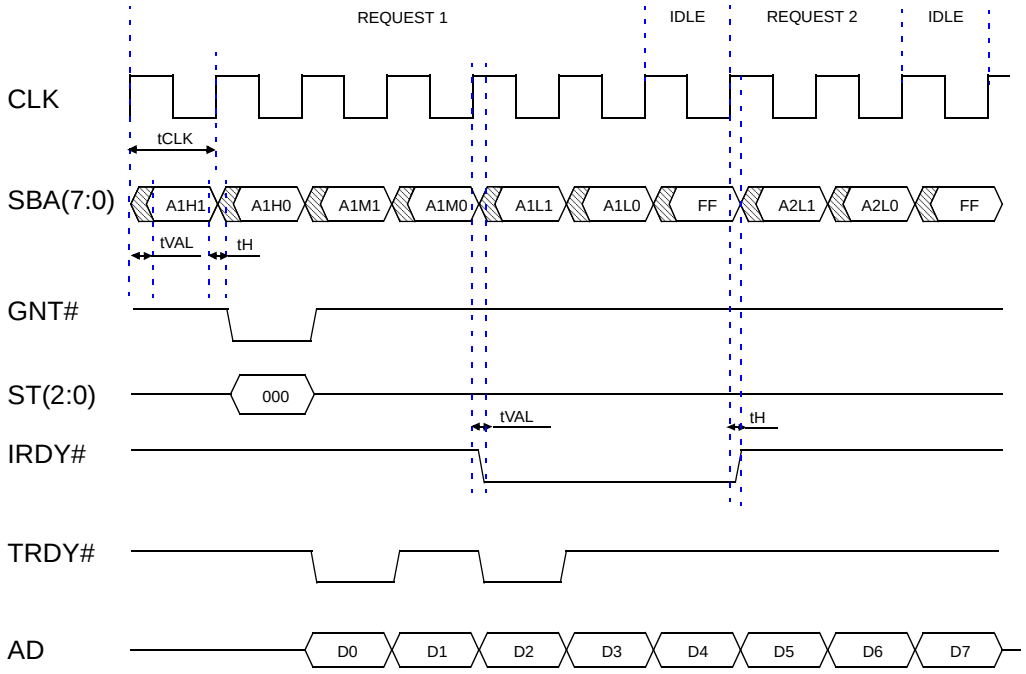


Figure 5-5. AGP 1X Read Request with Return Data (4 Qw)

Table 5-2 AGP 1X Timing Parameters

Symbol	Description	Minimum, ns	Maximum, ns
t_{clk}	CLK cycle time	15	30
t_{high}	CLK high time	6	
t_{low}	CLK low time	6	
t_{lock}	PLL lock time		1
t_{valc}	CLK to control signal valid delay	1	5.5
t_{vald}	CLK to data valid delay	1	6
t_{on}	Float to active delay	1	6
t_{off}	Active to float delay	1	14
t_{suc}	Control signals setup time to CLK	6	

Table 5-2 AGP 1X Timing Parameters

Symbol	Description	Minimum, ns	Maximum, ns
t_{sud}	DATA setup time to CLK	5.5	
t_h	Control signals hold time to CLK	0	

Note: In AGP 2X mode, the tvald, tsud and th values for AD. C/BEb and SBA signals are superseded by the AGP 2X parameters mentioned in *Table 5-3*

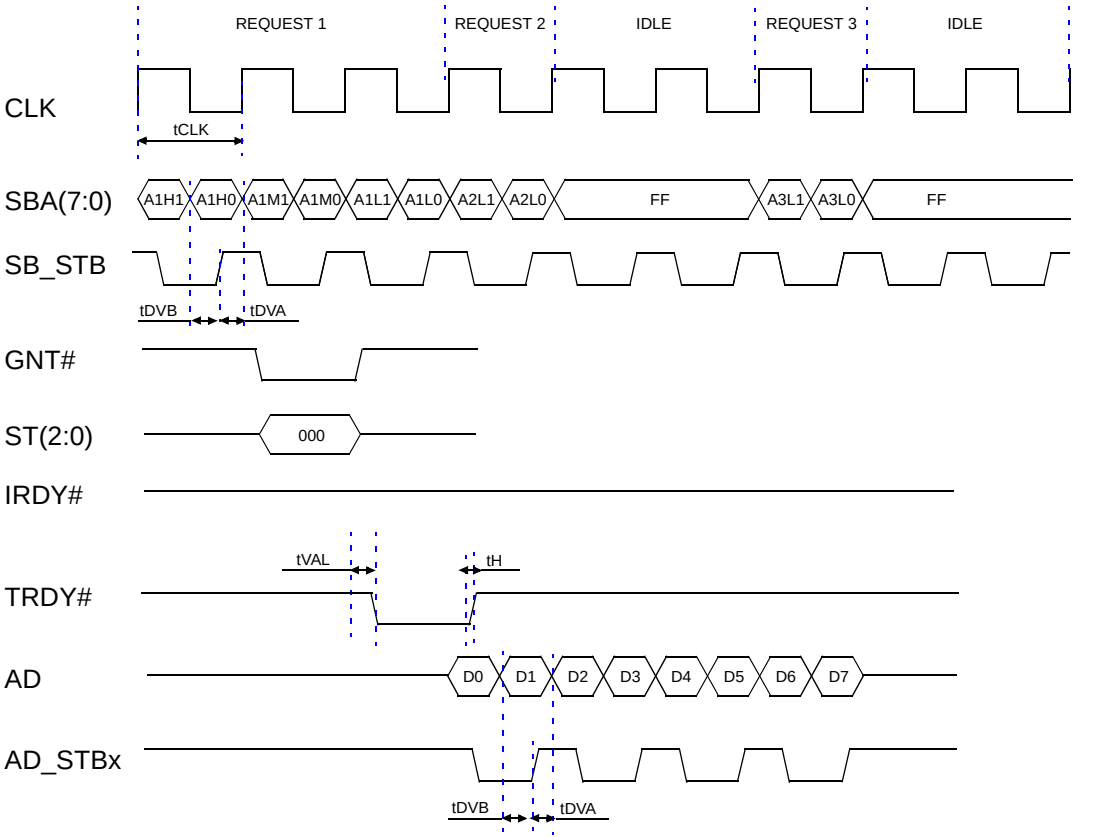


Figure 5-6. AGP 2X Read Request with Return Data (4Qw)

Table 5-3 AGP 2X Timing Parameters

Symbol	Description	Min, ns	Max, ns
tCLK	Clock		15
tDVB	Data valid before	1.7	
tDVA	Data valid after	1.7	
tVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	

5.1.6 Power-up and Reset Timing

The assertion and deassertion of the **RST#** signal is asynchronous with respect to clock. After **RST#** is asserted, **PCI** components must asynchronously float their outputs. Meeting both T_rst and T_rst-clk will be considered as proper reset of the internal logic for start-up of the chip.

Table 5-4 Reset Timing Parameters

Symbol	Parameter	Min	Max	Units
T_rst	Reset Active Time After Power Stable	1		ms
T_cyc	First Cycle after Reset	300		ns
T_rst-clk	Reset Active Time After CLK Stable	100		µs

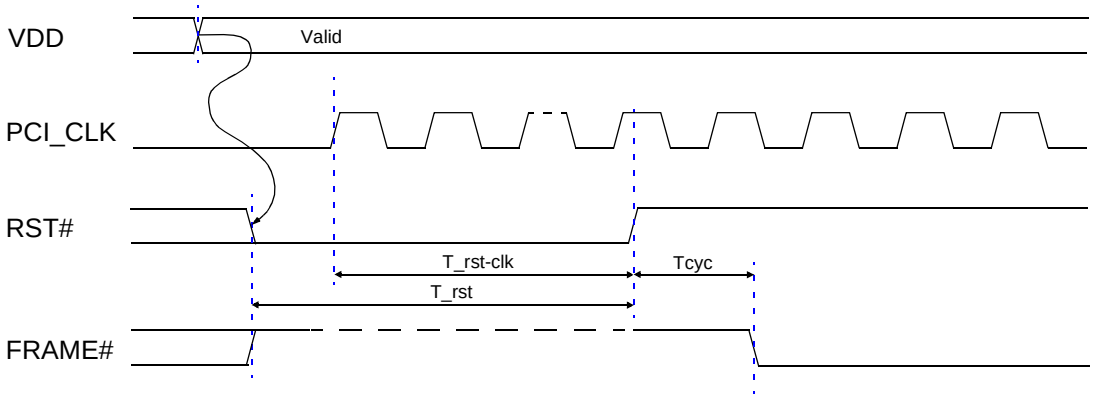


Figure 5-7. Reset Timing

5.2 Memory Timing

The following paragraph presents Timing specifications for SDRAM and SGRAM memory operations are given by:

- Refresh Cycle Timing, see *Figure 5-7*.
- SDRAM/SGRAM Cycle Timing, see *Figure 5-8*.

5.2.1 SDRAM/SGRAM Cycle Timing

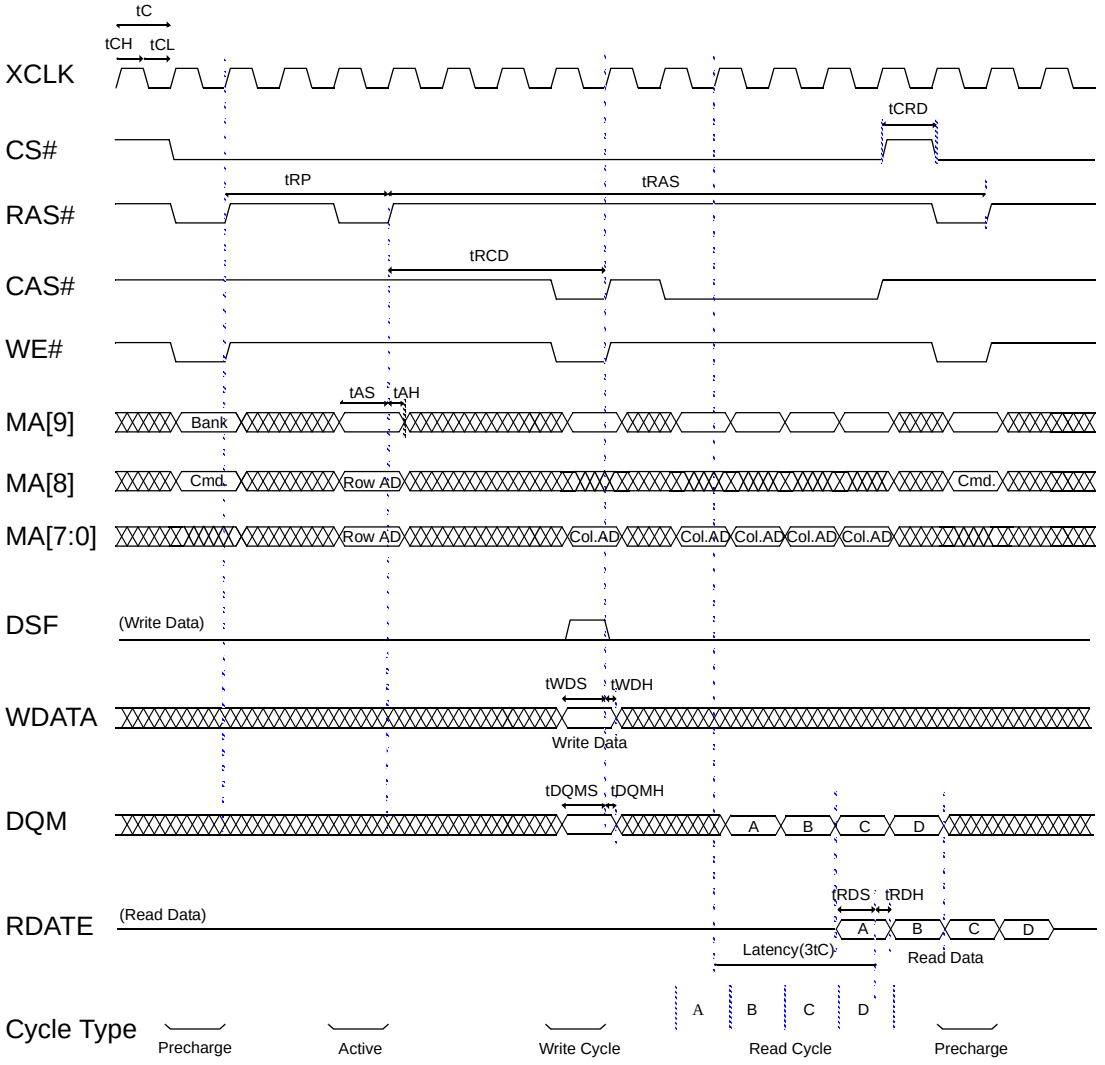


Figure 5-8. SDRAM / SGRAM Cycle Timing

Table 5-5 SDRAM/SGRAM Cycle Timing Values

Parameter	Symbol	Min, ns	Max, ns	Register in MEM_CNTL
Clock period	t_C	10	20	
Clock high time	t_{CH}	4.0		

Table 5-5 SDRAM/SGRAM Cycle Timing Values (Continued)

Parameter	Symbol	Min, ns	Max, ns	Register in MEM_CNTL
Clock low time	t_{CL}	3.5		
Command setup time provided (RAS, CAS, WE, CS, DSF)	t_{CMS}	5.0		
Command hold time provided (RAS, CAS, WE, CS, DSF)	t_{CMH}	1.3		
DQM setup time provided	t_{DQMS}	5.5		
DQM hold time provided	t_{DQMH}	1.2		
Address setup time provided	t_{AS}	4.4		
Address hold time provided	t_{AH}	1.3		
Write data setup time provided	t_{WDS}	3.0		
Write data hold time provided	t_{WDH}	2.1		
Read data setup time required	t_{RDS}	-0.9		
Read data hold time required	t_{RDH}	3.0		
Row cycle time	t_{RC}	2 t_C	12 t_C	MEM_TRP + MEM_TRAS
PRE to ACTV delay	t_{RP}	1 t_C	4 t_C	MEM_TRP[9:8]
ACTV to PRE min delay	t_{RAS}	1 t_C	8 t_C	MEM_TRAS[18:16]
ACTV to CMD delay	t_{RCD}	1 t_C	4 t_C	MEM_TRCD[11:10]
Write recovery time	t_{WR}	1 t_C	2 t_C	MEM_TCRD[12] + 1
ACTV to ACTV delay	t_{RRD}	2 t_C		
Block write cycle time	t_{BWC}	2 t_C		

Notes:

- Worst case numbers (max values) achieved assuming worst case process (setup time): 70 ^{o}C, 3.0 V, 45 pF on address and command lines, 30 pF on data and DQM lines.
- Best case number (min values) achieved assuming best case process (hold time): 0 ^{o}C, 3.6 V, 5 pF on address and command lines, 3.5 pF on data and DQM lines.
- Hold and setup time values considered without taking into account transmission line effects of the clock, address, command, data and DQM lines.
- Timing values are provided assuming 1.4 V transition level.

5.2.2 Memory Controller Register Programming Examples

SGRAM

Table 5-6 SGRAM (Samsung KM4132G512-8), XCLK Speed = 125 MHz, CAS Latency = 3

Parameter	SGRAM Specification, ns	Register Field in MEM_CNTL	Number of XCLKs	Time Provided, ns
Row cycle time	t_{RC} = 72, min	t_{RP} + t_{RAS}	9	72
PRE to ACTV delay	t_{RP} = 24, min	MEM_TRP = 10	3	24
ACTV to PRE min. delay	t_{RAS} = 48, min	MEM_TRAS = 101	6	48
ACTV to CMD delay	t_{RCD} = 16, min	MEM_TRCD = 10	2	16
Write recovery time	t_{WR} = 16, min	(MEM_TCRD=1) + 1	2	16

Table 5-7 Additional MEM_CNTL Register Bits to be Programmed

MEM_CNTL Bits	Register Field Name	Value
5:4	MEM_LATENCY	11 (4 clocks, SGRAM CAS latency 3)
19	MEM_REFRESH_DIS	0 (enabled)
23:20	MEM_REFRESH_RATE	1100 (1 every 1953 XCLK or 2048 cycles per 32ms for 125 MHz operation)

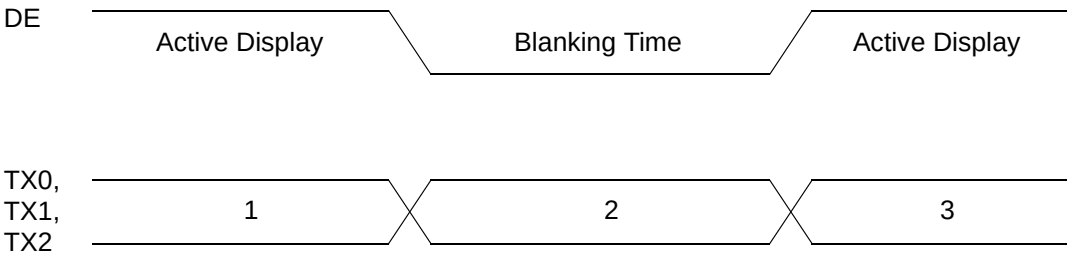
Table 5-8 Additional EXT_MEM_CNTL Register Bits to be Programmed

EXT_MEM_CNTL Bits	Register Field Name	Value
0	MEM_TBWC	1 (2 clocks per block-write)
9:8	MEM_SELECT	00 (SDRAM/SGRAM clock from DLL)
11:10	MEM_CAS_LATENCY	11 (SD/SGRAM CAS latency = 3 clocks)
27:24	MEM_GCMRS	0101

5.3 TMDS Timing

5.3.1 TMDS Transmission

- Takes parallel data and transmits it serially at high speed up to 1.12 Gbps per channel. It supports up to XGA (1024x768) with true color (16.7 million) for TFT panels at 60 Hz refresh.
- Uses 3 differential data pairs with timing and control data embedded in data transmission.
- Uses transition controlled binary DC-balanced coding for reliable, low-power, reduced EMI, and high-speed data transmission.
- Uses low-swing differential voltage.



1 - Transition Minimized, DC-Balanced Encoded Data
2 - Transition Maximized, DC-Balanced Encoded Data with Embedded Control Signals
3 - Transition Minimized, DC-Balanced Encoded Data

Figure 5-9. TMDS Transmission Timing Diagram

5.3.2 TMDS Data/Clock Mapping

The encoder is required to encode 8-bits of data during active display time and display enable (DE) + 2-bits of control signals during blank time. The encoding is required to generate 10-bit DC-balanced and transition-minimized codes during active display time. Control signals are assumed to change only during blank time when DE is low and their levels should be constant during active data period when DE is high. The diagram below shows the timing relation between DE and the transmitted graphic data at the output of LCD Controller. TXC indicates TMDS clock while TX0 to TX2 indicate the TMDS data channels. Since the TMDS differential clock is used only as a frequency reference to the internal PLL within the receiver, its phase relationship with the TMDS differential data would be irrelevant.

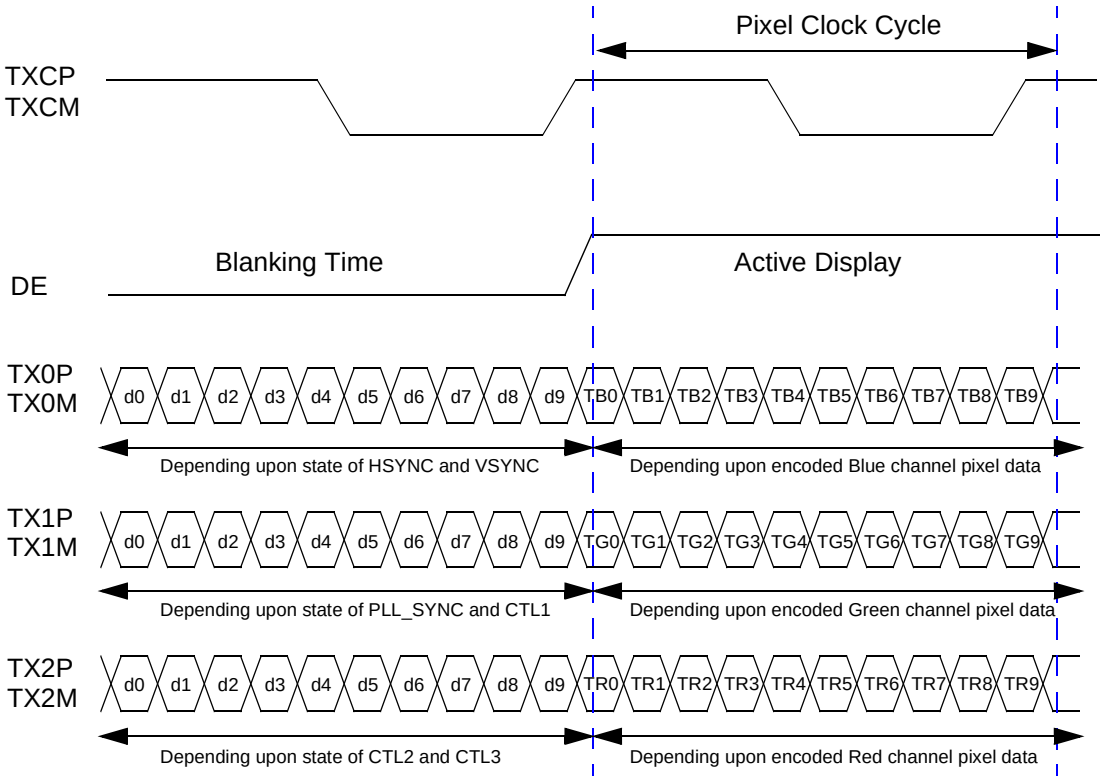


Figure 5-10. Encoded Timing Diagram for All Differential Data Pairs

Table 5-9 Pin/Signal Definition

Pin/Signal	Definition
TB0 - TB9	TMDS Transmitter Encoded Blue Channel Input (digital)
TG0 - TG9	TMDS Transmitter Encoded Green Channel Input (digital)
TR0 - TR9	TMDS Transmitter Encoded Red Channel Input (digital)
TXCP / TXCM	TMDS Positive / Negative Differential Transmitter Output Clock (analog)
TX0P / TX0M	TMDS Positive / Negative Differential Transmitter Output For Blue (analog)
TX1P / TX1M	TMDS Positive / Negative Differential Transmitter Output For Green (analog)
TX2P / TX2M	TMDS Positive / Negative Differential Transmitter Output For Red (analog)
QE23 - QE0	TMDS Receiver Even Output (digital)
QO23 - QO0	TMDS Receiver Odd Output (digital)
DE	Display Enable
HSYNC,VSYNC	Horizontal Sync and Vertical Sync
CTL1 - CTL3	TMDS Control data to be programmed by the user
CLK	TMDS Receiver Output Clock

Table 5-10 TMDS Out-of-Band Patterns

HSYNC/ PLL_SYNC/ CTL2	VSYNC/ CTL1/CTL3	d0	d1	d2	d3	d4	d5	d6	d7	d8	d9
0	0	0	0	1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	1	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1	0
1	1	1	1	0	1	0	1	0	1	0	1

Chapter 6
Electrical and Physical Data

6.1 Electrical Characteristics

6.1.1 Maximum Rating Conditions

These are stress ratings only. Operation of the device at these conditions is not recommended — prolonged exposure to absolute maximum rating conditions may affect the device reliability; any stress **greater** than the maximum ratings may cause permanent damage to the device.

Table 6-1 Maximum Rating Conditions

Item	Value
Supply Voltage, VDDC, VDDR	-0.50 V to +6.00 V
Supply Voltage, VDDP	-0.50 V to +6.00 V
Input or Output Voltage	-0.05 V to (VEE_{MAX} + 0.05 V)
DC Forward Bias Current	-12 mA (source), + 24 mA (sink)
Storage Temperature (Plastic)	-40 °C to 150 °C

6.1.2 Recommended DC Operating Conditions

Table 6-2 Recommended DC Operating Conditions

Item	Value
Operating Supply Voltage (VDDC)	2.5 V
Operating Supply Voltage (VDDR)	3.3 V
Operating Supply Voltage (VDDP)	3.3 V
Operating Case Temperature (TC)	Refer to *Table 6-14 on page 6-13*

6.1.3 AC Characteristics

General

Table 6-3 AC Characteristics - General Interface

Signals	Typical Capacitive Load *
ROMCS#	10 pF
AD[31:0], DEVSEL#, TRDY#, STOP#, INTR#, PAR	50 pF
AMC	25 pF
HSYNC, VSYNC	50 pF
CAS, MD[63:0], RAS, CS[3:0]	25 pF
WE[7:0]	15 pF
MA[9:0]	45 pF

* 4MB, 256Kx16 DRAMs, through a PCI edge connector.

TMDS

Table 6-4 AC Characteristics - TMDS (normal operating conditions)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{CIP}	Clock Period		40		8.9	ns
F_{CIP}	Frequency		25		112	MHz
S_{LHT}	Small Swing Low-to-High Transition Time	C_{LOAD} = 5 pF	0.25	0.3	0.5	ns
S_{HLT}	Small Swing High-to-Low Transition Time	C_{LOAD} = 5 pF	0.25	0.3	0.5	ns

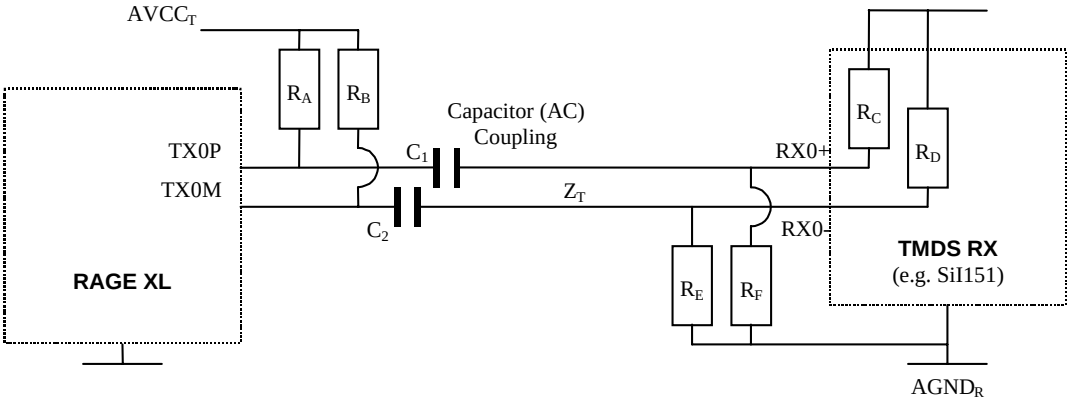


Figure 6-1. Capacitor Coupling between TMDS TX and RX.

Table 6-5 Component Values for Capacitor Coupling

Component	Value	Comment
Z_T	100 Ω	Transmission cable
C_1, C_2	10 nF ± 20%	Capacitors on Transmitter end
R_A, R_B	100 Ω	Maintain DC current in current source of transmitter
R_C, R_D	50 Ω	Internal termination resistors of receiver
R_E, R_F	180 Ω	Maintain DC voltage of $AVCC_R$-V_{OD} at RX0+ and RX0-

6.1.4 DC Characteristics

TTL Interface

Table 6-6 TTL DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{OL}	Low Level Output Voltage	I_{OL}=Rated Buffer Current	-	0.2	0.4	V
V_{OH}	High Level Output Voltage	I_{OH}=Rated Buffer Current	2.4	3.3		V

TMDS Interface

Table 6-7 TMDS DC Characteristics (normal operating conditions)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TXVDDR	Supply Voltages		2.375	2.50	2.625	V
TXVSSR	Ground		0.0	0.0	0.0	V
V_{OD}	Differential Output Voltage Single ended peak to peak amplitude	R_{LOAD} = 50Ω R_{SWING} = 850Ω R_{SWING} = 680Ω R_{SWING} = 400Ω	 250 310 580	 300 370 650	 350 430 720	 mV mV mV

Note: R_{SWING} is set by programming internal register PPPVS [3:0] which can select resistance from 400Ω to 850Ω step.

General

Table 6-8 DC Characteristics - General Interface

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
I_{IL}	Low level Input Current	V_I = VSS	-	-	+1	µA
I_{IH}	High Level Input Current	V_I = VDD	-	-	-1	µA
I_{OZ}	Tri-State Output Leakage	VO = 0 V or VDD	-	-	±10	µA
C_{IN}	Input Capacitance	Freq = 1 MHz @ 0 V	-	4	6	pF
C_O	Output Capacitance	Freq = 1 MHz @ 0 V	-	6	-	pF
C_{IO}	Bidirectional I/O Capacitance	Freq = 1 MHz @ 0 V	-	6	10	pF
I_{KLU}	I/O Latch-up Current	V < VSS, V > VDD	100	-	-	mA
V_{EPO}	Electrostatic Protection	C = 100 pF, R = 1.5 KΩ	2000	-	-	V

6.1.5 Input/Output Specifications

Table 6-9 Input/Output Electrical Specifications

Pin Name	Type	I_{OL}(min), mA	I_{OH}(min), mA	Internal PU/PD[1]	Tri-State	Interface Level
AD[31:0]	I/O	4	-4			3.3 V / 5 V
C/BE[3:0]#	I/O	18	-18			3.3 V / 5 V
CPUCLK	I					3.3 V / 5 V
DEVSEL#	I/O	18	-18		Yes	3.3 V / 5 V
FRAME#	I/O	18	-18		Yes	3.3 V / 5 V
IDSEL	I					3.3 V / 5 V
INTR#	O	18	-18		Yes	3.3 V / 5 V
IRDY#	I/O	18	-18		Yes	3.3 V / 5 V
PAR	O	18	-18		Yes	3.3 V / 5 V
RESET#	I					3.3 V / 5 V
STOP#	I/O	18	-18		Yes	3.3 V / 5 V
TRDY#	I/O	18	-18		Yes	3.3 V / 5 V
REQ#	O	18	-18		Yes	3.3 V / 5 V
GNT#	I					3.3 V / 5 V
CAS#	I/O	16	-16	50K PD	Yes	3.3 V, 5 V Tol.
MA[11:0]	I/O	8	-8	50K PD	Yes	3.3 V, 5 V Tol.
MD[63:0]	I/O	2	-2	50K PD	Yes	3.3 V, 5 V Tol.
HCLK	I/O	16	-16	50K PU	Yes	3.3 V, 5 V Tol.
WE#	I/O	16	-16	50K PU	Yes	3.3 V, 5 V Tol.
CKE	I/O	16	-16	50K PU	Yes	3.3 V, 5 V Tol.
ROMCS#	I/O	4	-4		Yes	3.3 V, 5 V Tol.
DSF	I/O	8	-8		Yes	3.3 V, 5 V Tol.
RAS#	I/O	16	-16	50K PU	Yes	3.3 V, 5 V Tol.
DQM[7:0]	I/O	16	-16	50K PU	Yes	3.3 V, 5 V Tol.
CS[1:0]	I/O	16	-16	50K PU	Yes	3.3 V, 5 V Tol.
R, G, B	A					
RSET	A					
HSYNC	O	8	-8		Yes	3.3 V, 5 V Tol.
VSYNC	O	8	-8		Yes	3.3 V, 5 V Tol.
XTALIN	I					3.3 V, 5 V Tol.
XTALOUT	O					

Table 6-9 Input/Output Electrical Specifications (Continued)

Pin Name	Type	I_{OL}(min), mA	I_{OH}(min), mA	Internal PU/PD[1]	Tri-State	Interface Level
AS	I/O	8	-8		Yes	3.3 V, 5 V Tol.
BYTECLK	I/O	8	-8		Yes	3.3 V, 5 V Tol.
DS	I/O	8	-8		Yes	3.3 V, 5 V Tol.
DVS[7:0]	I			50K PU		3.3 V, 5 V Tol.
DVSCLK	I					3.3 V, 5 V Tol.
SDA	I/O	8	-8		Yes	3.3 V, 5 V Tol.
SCL	I/O	8	-8		Yes	3.3 V, 5 V Tol.
SAD[7:0]	I/O	8	-8		Yes	3.3 V, 5 V Tol.
SRDY / IRQ	I/O	8	-8		Yes	3.3 V, 5 V Tol.
DPFCLK	I/O	8	-8		Yes	3.3 V, 5 V Tol.
DPFDAT	I/O	8	-8		Yes	3.3 V, 5 V Tol.
MONDET	I					3.3 V, 5 V Tol.
MONID[3:0]	I/O	8	-8		Yes	3.3 V, 5 V Tol.
TESTEN	I					3.3 V, 5 V Tol.
ST[2:0]	I	8	-8		Yes	3.3 V
SBA[7:0]	O	8	-8		Yes	3.3 V
AD_STB[1:0]	I/O	8	-8		Yes	3.3 V
SB_STB[1:0]	O	8	-8		Yes	3.3 V
PCI33EN	I					3.3 V, 5 V Tol.
TXCP	A	See Table 6-10 below				
TXCM	A					
TX0P	A					
TX0M	A					
TX1P	A					
TX1M	A					
TX2P	A					
TX2M	A					

1. Although RAGE XL contains internal pull-up and pull-down resistors, external pull-up/pull-down resistor straps are required as described in section 3.10 to ensure proper initialization of the ASIC for all implementations.

Table 6-10 Transmitter Electrical Specifications

Output Voltage	Value
Single-ended high level output, V_H	AV_{CC}
Single-ended low level output, V_L	AV_{CC} - 600mV
Single-ended output swing, V_{swing}	600mV
Single-ended standby (off) output, V_{OFF}	AV_{CC}

Note: AV_{CC} is the supply voltage of the TMDS receiver, 3.3V +/- 10%

6.1.6 DAC Characteristics

All voltages in the table below are referenced to VSS unless specified otherwise.

The Pixel Clock frequency must be stable for a period of at least 20 seconds after power up (or after a change in Pixel Clock frequency), before proper device operation characteristics are guaranteed.

Table 6-11 DAC Characteristics*

Symbol	Parameter	Min	Typ	Max	Unit	Notes
-	Resolution	8	-	-	bits	A
V_O(max)	Maximum Output Voltage	1.1	-	-	V	A
I_O(max)	Maximum Output Current	-	22.05	-	mA	A
-	Full Scale Error	-10	-	+10	%	B, C
-	DAC to DAC Correlation	-2	-	+2	%	A, D
-	Integral Linearity	-0.5	-	0.5	LSB	A, E
-	Rise Time (10% to 90%)	-	-	3	ns	A, F
-	Full Scale Settling Time	-	8	-	ns	A, G, H
-	Glitch Energy	-	60	-	pV-S	A, H
-	Monotonicity	-	-	-	-	I
V_{REFM}	Measured Reference Voltage	-6%	1.235	+6%	V	J

Notes:

A. Tested over the operating temperature range, at nominal supply voltage with an IREF of -2.93 mA. IREF is the level of the current flowing in the RSET resistor.

B. Tested over the operating temperature range, at reduced supply voltage, with a -2.93 mA IREF. IREF is the level of the current flowing in the RSET resistor.

C. Full scale error from the value predicted by the design equations.

D. About the mid point of the distribution of the three DAC's measured at full scale deflection.

E. Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

F. Load = 37.5Ω + 20 pf with IREF = -2.93 mA. (IREF is the current flowing in the RSET resistor).

G. From a 2% change in the output voltage until settling to within 2% of the final value.

H. This parameter is sampled, not 100% tested.

I. Monotonicity is guaranteed.

J. V_{REFM} is the measured value of logged data. It is the idealized V_{REF} shifted by 2.9%.

6.1.7 Calculating RSET Resistance (DAC Interface)

A precision resistor (with 1% of nominal) is placed between RSET (pin 123) and analog ground (AVSS) to set the full-scale DAC current. This resistance is typically 365Ω for PS/2 applications where the effective impedance is 37.5Ω (doubly terminated 75Ω loads, shown in the following figure). 365Ω is an acceptable value for RSET with a slightly reduced white level.

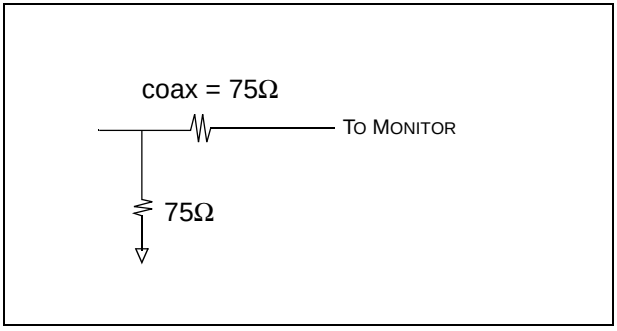


Figure 6-2. PS/2 Example

The required value for the RSET resistor was calculated using the following formula:

RSET (Ω) = (6.22 x Vref x *a*)/ Iout

where:

- 6.22 is the idealized 8-bit gain constant.

- Vref is the idealized reference voltage (1.2V).

- *a* is the empirically determined systematic composite skew on idealized Vref and gain constant.

- Iout is the required DAC full-scale current given by:

Iout = (Vwhite - Vblack) / Zeff

Since Vwhite = 0.7V, Vblack = 0V, Zeff = 37.5Ω

Iout = (0.7V - 0V) / 37.5Ω = 0.0186A

Defining RSET in this fashion allows for a one time compensation for the systematic skew due to shifts on both Vref and the gain constant on the output white level by adjustment of *a*.

Example: Calculating the value of RSET for PS/2 application:

RSET = (6.22 x Vref x *a*) / Iout = 6.22 x 1.2 x 0.91/ 0.0186 = 365Ω

Note: The above calculation for the RSET resistor is for illustration purpose only, even though it gives the correct recommended value (by virtue of using the correct *a*) . Do not attempt to calculate the RSET value for your application. **Always contact the FAE Department of ATI to check the latest recommended value for RSET.**

6.1.8 Analog Output Specification

Conceptually, each 8-bit DAC can be viewed as two current sources connected in parallel. Each current source is controlled independently as shown below.

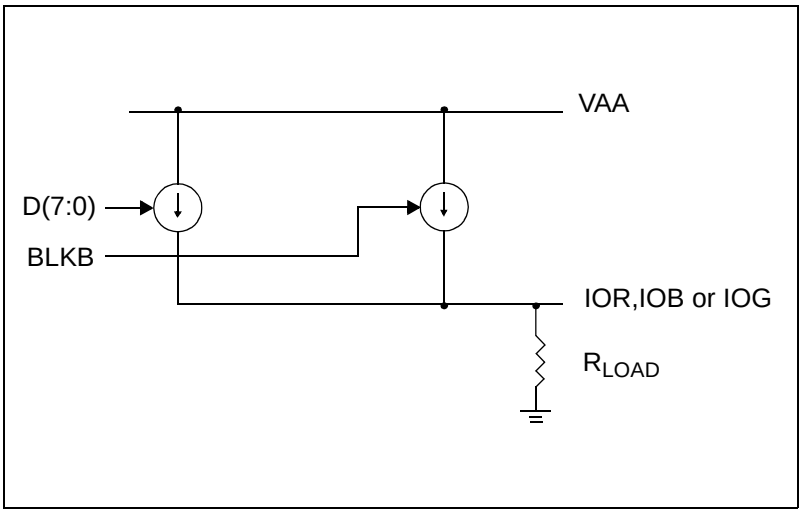


Figure 6-3. Analog Output (DAC)

With a 75 Ω doubly-terminated load, VREF = 1.2 V, and RSET = 397 Ω PS/2 levels are shown below, with pedestal current set to 7.5 IRE.

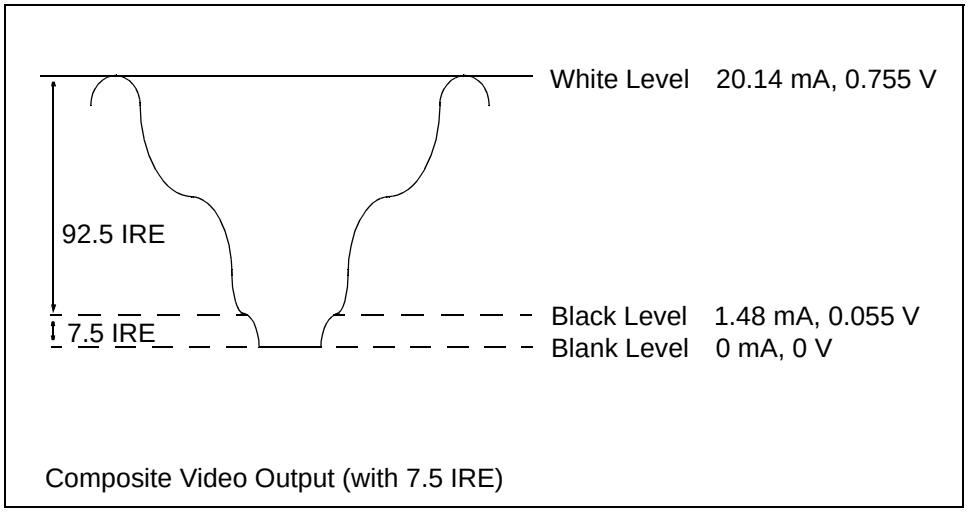


Figure 6-4. Analog Output (Composite)

6.2 Thermal Characteristics

6.2.1 Maximum Ambient Temperature

The thermal operating characteristics of the chip depend on the board it is mounted on. Typical maximum ambient temperatures ($T_A max$) can be derived from the following equation:

$$T_A max = T_C max - P * \theta_{CA}$$

where $T_C max$ - maximum case temperature,
P - power dissipation,
θ_{CA} - case-to-ambient thermal resistance.

Power dissipation varies with different display modes but is typically between 1.0 W to 2.0 W when the chip is operating at nominal VDD. Case temperature (T_C) is taken at the center of the top surface of the device.

The table below shows typical values of θ_{CA} and $T_A max$ for different airflows over the RAGE XL.

Table 6-12 Thermal Characteristics versus Air Flow

Airflow (m/s)	θ_{CA} (°C/W)	$T_A max$ (°C)
0	21	68
1.0	17.7	62
2.0	13.7	54

6.2.2 Maximum Recommended Junction and Case Temperature

The junction-to-case thermal resistance (θ_{JC}) of this device is approximately 3 °C/W. Junction temperature (T_J) and Case temperature (T_C) may be calculated as follows:

$$T_J = (\theta_{JC} + \theta_{CA}) * P + T_A$$

$$T_C = \theta_{CA} * P + T_A$$

Table 6-13 RAGE XL Thermal Characteristics

Variable	Value
Ambient operating temperature range	+10°C to +50°C
Maximum allowable case temperature	85°C

Table 6-13 RAGE XL Thermal Characteristics

Variable	Value
Maximum allowable junction temperature	100°C

6.2.3 Board Power and Case Temperature Measurements

The following table represents the results of RAGE XL ASIC and memory (8M SDRAM) power consumption and ASIC case temperature measurements, carried out at a room temperature of 24°C with no CPU fan air flow. An Intel VC820 motherboard with Pentium III 450 MHz was used as a test station. The measurement tolerance allowed was ± 5%.

For the measurements, the test system configuration was as follows: RAGE XL B41, 109-66900-10A, AGP, BIOS: 4.027, 8M SDRAM. The display device used was a Sony Multiscan 15sf ll.

Test Results - 125 MHz Mem clock / 83 MHz Eng clock (2:1):

Table 6-14 Average Power Dissipation

Display Mode	Pattern/test	12V Power (W)	5V Power (W)	3.3V Power (W)	VDDQ Power (W)	Total Board Power (W)	Core Power (W)	ASIC Case Temp. (C)
1024x768, 16bpp, 75Hz	Static-Windows	0.02	0.34	1.06	0.002	1.42	0.69	45.74
1024x768, 16bpp, 75Hz	Winstone	0.02	0.34	1.09	0.03	1.49	0.71	47.09
1024x768, 16bpp, 120Hz	Incoming	0.02	0.38	1.92	0.05	2.36	1.18	57.53

Table 6-15 Maximum (Peak) Power Dissipation

Display Mode	Pattern/test	12V Power (W)	5V Power (W)	3.3V Power (W)	VDDQ Power (W)	Total Board Power (W)	Core Power (W)	ASIC Case Temp. (C)
1024x768, 16bpp, 75Hz	Winstone	0.08	0.37	1.53	0.05	2.03	0.89	47.55
1024x768, 16bpp, 120Hz	Incoming	0.08	0.43	2.30	0.07	2.88	1.47	59.14

6.3 Physical Dimensions

Package Outline PBGA 27x27mm, 256 +16 pins

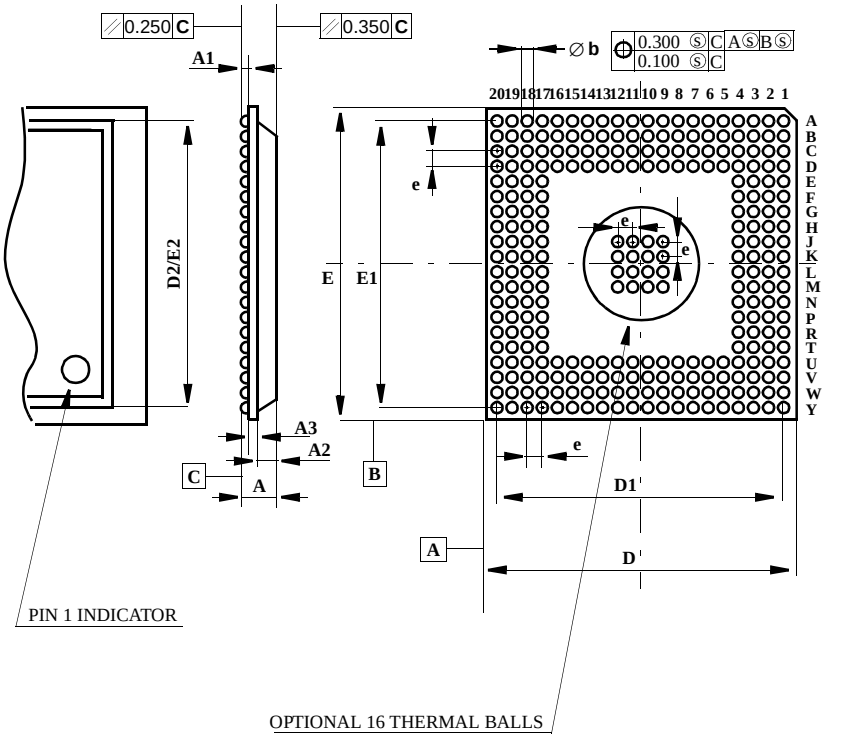


Figure 6-5. 272-pin PBGA Physical Dimensions

Table 6-16 272-Pin PBGA Package Physical Dimensions (in mm)

Reference	Typical	Min	Max
A	2.13	1.93	2.33
A1	0.60	0.50	0.70
A2	1.17	1.12	1.22
A3	0.36	0.31	0.41
b	0.75	0.60	0.90
D	27.00	26.80	27.20
D1	24.13 BASIC	-	-
D2	24.00	23.90	24.10
e	1.27 BASIC	-	-
E	27.00	26.82	27.18
E1	24.13 BASIC	-	-
E2	24.13 BASIC	-	-

6.4 Environmental Requirements

6.4.1 Storage Temperature

Maximum storage temperatures allowed are -40 °C and 150 °C

6.4.2 Relative Humidity

Operation: 5% to 90% non-condensing

Storage: 0% to 95%

This page intentionally left blank.

Chapter 7
Display Modes

The RAGE XL is capable of a wide variety of modes for CRT and LCD outputs. This chapter describes the modes supported and their respective memory requirements.

NOTE: In all cases, memory configuration is assumed to be 100 MHz SGRAM.

7.1 2D Modes

The following table shows the 2D modes supported for both CRT and LCD. The table specifies the minimum memory requirement for various display resolutions, refresh rates and color depths.

Table 7-1 2D Modes (TFT or CRT)

Mode	Refresh Rate (Hz)	Minimum Amount of Memory Required			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60	2 MB	2 MB	2 MB	2 MB
640x480	72	2 MB	2 MB	2 MB	2 MB
640x480	75	2 MB	2 MB	2 MB	2 MB
640x480	90	2 MB	2 MB	2 MB	2 MB
640x480	100	2 MB	2 MB	2 MB	2 MB
800x600	60	2 MB	2 MB	2 MB	4 MB
800x600	70	2 MB	2 MB	2 MB	4 MB
800x600	75	2 MB	2 MB	2 MB	4 MB
800x600	90	2 MB	2 MB	2 MB	4 MB
800x600	100	2 MB	2 MB	2 MB	4 MB
1024x768	60	2 MB	2 MB	4 MB	4 MB
1024x768	72	2 MB	2 MB	4 MB	4 MB
1024x768	75	2 MB	2 MB	4 MB	4 MB
1024x768	90	2 MB	2 MB	4 MB	4 MB
1024x768	100	2 MB	2 MB	4 MB	4 MB

Table 7-1 2D Modes (TFT or CRT) (Continued)

Mode	Refresh Rate (Hz)	Minimum Amount of Memory Required			
		8 bpp	16 bpp	24 bpp	32 bpp
1280x1024	43	2 MB	4 MB	4 MB	6 MB
1280x1024	60	2 MB	4 MB	4 MB	6 MB
1280x1024	70	2 MB	-	4 MB	6 MB
1280x1024	72	2 MB	-	4 MB	6 MB
1600x1200	60	4 MB	4 MB	6 MB	8 MB
1600x1200	66	4 MB	4 MB	6 MB	8 MB
1600x1200	76	4 MB	4 MB	6 MB	-
1600x1200	85	4 MB	4 MB	6 MB	-
	Shading indicates modes not supported by TFT				

7.2 Full Screen 3D Modes

The following table shows the minimum memory requirements for full screen 3D display in various colour depths and resolutions.

Table 7-2 Full Screen 3D Modes (TFT or CRT)

Mode	Refresh Rate (Hz)	Min Req Memory with Z Buffer Enabled				Min Req Memory with Z Buffer Disabled			
		8 bpp	16 bpp	24 bpp	32 bpp	8 bpp	16 bpp	24 bpp	32 bpp
640x480	60	2 MB	2 MB	4 MB	4 MB	2 MB	2 MB	2 MB	4 MB
640x480	72	2 MB	2 MB	4 MB	4 MB	2 MB	2 MB	2 MB	4 MB
640x480	75	2 MB	2 MB	4 MB	4 MB	2 MB	2 MB	2 MB	4 MB
640x480	90	2 MB	2 MB	4 MB	4 MB	2 MB	2 MB	2 MB	4 MB
640x480	100	2 MB	2 MB	4 MB	4 MB	2 MB	2 MB	2 MB	4 MB
800x600	60	4 MB	4 MB	4 MB	6 MB	2 MB	2 MB	4 MB	4 MB
800x600	70	4 MB	4 MB	4 MB	6 MB	2 MB	2 MB	4 MB	4 MB
800x600	75	4 MB	4 MB	4 MB	6 MB	2 MB	2 MB	4 MB	4 MB
800x600	90	4 MB	4 MB	4 MB	6 MB	2 MB	2 MB	4 MB	4 MB
800x600	100	4 MB	4 MB	4 MB	6 MB	2 MB	2 MB	4 MB	4 MB
1024x768	60	4 MB	6 MB	8 MB	8 MB	2 MB	4 MB	6 MB	8 MB
1024x768	72	4 MB	6 MB	8 MB	8 MB	2 MB	4 MB	6 MB	8 MB
1024x768	75	4 MB	6 MB	8 MB	8 MB	2 MB	4 MB	6 MB	8 MB
1024x768	90	4 MB	6 MB	8 MB	8 MB	2 MB	4 MB	6 MB	8 MB
1024x768	100	4 MB	6 MB	8 MB	8 MB	2 MB	4 MB	6 MB	8 MB
1280x1024	43	6 MB	8 MB	-	-	4 MB	6 MB	8 MB	-
1280x1024	60	6 MB	8 MB	-	-	4 MB	6 MB	8 MB	-
1280x1024	70	6 MB	8 MB	-	-	4 MB	6 MB	8 MB	-
1280x1024	72	6 MB	8 MB	-	-	4 MB	6 MB	8 MB	-
1600x1200	60	8 MB	-	-	-	4 MB	8 MB	-	-
1600x1200	66	8 MB	-	-	-	4 MB	8 MB	-	-
1600x1200	76	8 MB	-	-	-	4 MB	8 MB	-	-
1600x1200	85	8 MB	-	-	-	4 MB	8 MB	-	-
	Shading indicates modes not supported by TFT								

7.3 DVD/Video Modes

The following two tables show memory requirements for DVD Video Playback for both software and hardware MPEG decoding in various display modes. Both NTSC and PAL formats are provided in each table. DVD NTSC is a 720x480 YUV mode running at 30 frames per second. DVD PAL is a 720x576 YUV mode running at 25 frames per second. The YUV mode is YUV12 in software MPEG decoding and YUV422 in hardware MPEG decoding.

7.3.1 Software MPEG Decoding

Table 7-3 DVD Video Playback in a Window with Software MPEG Decoding

Mode	Refresh Rate (Hz)	Min Req Memory for DVD NTSC Format				Min Req Memory for DVD PAL Format			
		8 bpp	16 bpp	24 bpp	32 bpp	8 bpp	16 bpp	24 bpp	32 bpp
640x480	60	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640x480	72	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640x480	75	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640x480	90	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640x480	100	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800x600	60	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	6 MB
800x600	70	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	6 MB
800x600	75	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	6 MB
800x600	90	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	6 MB
800x600	100	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	6 MB
1024x768	60	4 MB	4 MB	6 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024x768	72	4 MB	4 MB	6 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024x768	75	4 MB	4 MB	6 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024x768	90	4 MB	4 MB	6 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024x768	100	4 MB	4 MB	6 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1280x1024	43	4 MB	6 MB	6 MB	8 MB	4 MB	6 MB	8 MB	8 MB
1280x1024	60	4 MB	6 MB	6 MB	8 MB	4 MB	6 MB	8 MB	8 MB
1280x1024	70	4 MB	6 MB	6 MB	8 MB	4 MB	6 MB	8 MB	8 MB
1280x1024	74	4 MB	6 MB	6 MB	8 MB	4 MB	6 MB	8 MB	8 MB
1600x1200	60	-	-	-	-	8 MB	8 MB	-	-
1600x1200	66	-	-	-	-	8 MB	8 MB	-	-
1600x1200	76	-	-	-	-	8 MB	8 MB	-	-
1600x1200	85	-	-	-	-	8 MB	8 MB	-	-

Shaded areas indicate differences between NTSC and PAL formats. Note that TFT does not support 1280x1024 modes and beyond.

7.3.2 Hardware MPEG Decoding

Table 7-4 DVD Video Playback in a Window with Hardware MPEG Decoding

Mode	Refresh Rate (Hz)	Min Req Memory for DVD NTSC Format				Min Req Memory for DVD PAL Format			
		8 bpp	16 bpp	24 bpp	32 bpp	8 bpp	16 bpp	24 bpp	32 bpp
640x480	60	2 MB	2 MB	4 MB	4 MB	2 MB	4 MB	4 MB	4 MB
640x480	72	2 MB	2 MB	4 MB	4 MB	2 MB	4 MB	4 MB	4 MB
640x480	75	2 MB	2 MB	4 MB	4 MB	2 MB	4 MB	4 MB	4 MB
640x480	90	2 MB	2 MB	4 MB	4 MB	2 MB	4 MB	4 MB	4 MB
640x480	100	2 MB	2 MB	4 MB	4 MB	2 MB	4 MB	4 MB	4 MB
800x600	60	2 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800x600	70	2 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800x600	75	2 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800x600	90	2 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800x600	100	2 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
1024x768	60	4 MB	4 MB	4 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024x768	72	4 MB	4 MB	4 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024x768	75	4 MB	4 MB	4 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024x768	90	4 MB	4 MB	4 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1024x768	100	4 MB	4 MB	4 MB	6 MB	4 MB	4 MB	6 MB	6 MB
1280x1024	43	4 MB	4 MB	6 MB	8 MB	4 MB	6 MB	6 MB	8 MB
1280x1024	60	4 MB	4 MB	6 MB	8 MB	4 MB	6 MB	6 MB	8 MB
1280x1024	70	4 MB	4 MB	6 MB	8 MB	4 MB	6 MB	6 MB	8 MB
1280x1024	74	4 MB	4 MB	6 MB	8 MB	4 MB	6 MB	6 MB	8 MB
1600x1200	60	-	-	-	-	-	-	-	-
1600x1200	66	-	-	-	-	-	-	-	-
1600x1200	76	-	-	-	-	-	-	-	-
1600x1200	85	-	-	-	-	-	-	-	-

Shaded areas indicate differences between NTSC and PAL formats. Note that TFT does not support 1280x1024 modes and beyond.

This page intentionally left blank.

Chapter 8
NAND Tree Implementation

This chapter comprises the following:

- A brief explanation of a NAND tree.
- A truth table of a sample circuit.
- An ordered list of the pins in the NAND tree for the RAGE XL.
- The test modes used for RAGE XL.
- A description of the NAND tree mode testing procedure.
- The pins which are not included in the NAND tree.

8.1 Overview

This section details a brief description of a generic NAND tree. A sample of a NAND tree is shown in the figure below.

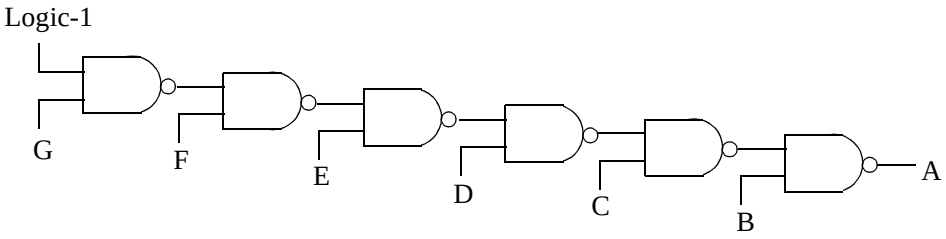


Figure 8-1. Sample of a NAND Tree

Pin A is assigned the output direction, and pins B through G are assigned the input direction. A logic ‘1’ is provided to the same NAND gate that pin G is driving. The output value or the truth table and, therefore, the test vector for this circuit is shown below. The ‘x’ values, in the lower left triangle of the table, represent ‘don't care’ values, and they are usually left at logic ‘0’ within a board test vector. Notice how the output value on pin A toggles between ‘0’ and ‘1’, as a logic ‘0’ is ‘walked’ through the truth table from left to right.

Table 8-1 NAND Tree Truth Table

G	F	E	D	C	B	A
1	1	1	1	1	1	1
0	1	1	1	1	1	0
x	0	1	1	1	1	1
x	x	0	1	1	1	0
x	x	x	0	1	1	1
x	x	x	x	0	1	0
x	x	x	x	x	0	1

8.2 NAND tree in RAGE XL

There is only one NAND tree in RAGE XL. The output pin is MD63. The order of the NAND tree pin connection is given in *Table 8-2* below.

NOTE: When generating vector, follow the order of the pins and force value transitions sequentially (e.g., force DVS7 to logic 0, observe MD63; force DVS6 to logic 0, observe MD63; …).

Table 8-2 RAGE XL NAND Tree listing (BGA 256-pin package)

Order	Signal Name	RAGE XL Pin Number	Order	Signal Name	RAGE XL Pin Number
1	DVS7	A3	24	SRDY	H3
2	DVS6	B3	25	I2CDATA	J3
3	DVS5	C3	26	I2CCLK	J2
4	DVS4	A2	27	MONID3	J4
5	DVS3	B2	28	MONID2	K3
6	DVS2	C2	29	MONID0	K1
7	DVS1	C1	30	HSY	M2
8	ROMCS#	D3	31	VSY	M3
9	DVS0	D1	32	SBA3	P3
10	DVSCLK	E1	33	SBA2	P2
11	MONDET	E4	34	SBA1	N3
12	MONID1	K2	35	SBA0	N2
13	SAD7	E2	36	SBA4	P1
14	SAD6	E3	37	ST0	T1
15	SAD5	F3	38	ST1	T3
16	SAD4	F1	39	ST2	R2
17	SAD3	F2	40	SB_STB	R1
18	SAD2	G3	41	INTR#	V3
19	SAD1	G2	42	GNT#	T2
20	SAD0	G1	43	REQ#	U1
21	BYTCLK	H1	44	RESET#	U2
22	DS	H2	45	CPUCLK	V1
23	AS	J1	46	AD31	W1

Table 8-2 RAGE XL NAND Tree listing (BGA 256-pin package) (Continued)

Order	Signal Name	RAGE XL Pin Number	Order	Signal Name	RAGE XL Pin Number
47	AD30	V2	80	AD10	Y13
48	AD29	Y1	81	AD9	V12
49	AD28	W2	82	CBE0#	V13
50	AD27	Y2	83	AD_STB0	W13
51	AD26	V3	84	AD8	Y14
52	AD25	Y3	85	AD7	W14
53	AD24	W3	86	AD6	V14
54	CBE3#	W4	87	AD5	Y15
55	AD_STB1	Y4	88	AD4	W15
56	SBA5	V5	89	AD3	Y16
57	SBA6	W6	90	AD2	V15
58	SBA7	V6	91	AD1	W16
59	AD23	Y5	92	AD0	V16
60	AD22	W5	93	PCI33EN	U16
61	AD21	Y6	94	CS0	W17
62	AD20	V7	95	CS1	Y17
63	AD19	Y7	96	MA10	U19
64	AD18	W7	97	MA11	U20
65	AD17	W8	98	MA0	Y18
66	AD16	V8	99	MA1	Y19
67	CBE2#	Y8	100	MA2	Y20
68	IRDY#	Y9	101	DFPDAT	V17
69	FRAME#	W9	102	MA3	W18
70	TRDY#	V9	103	MA4	W19
71	DEVSEL#	Y10	104	MA5	W20
72	CBE1#	W10	105	MA6	V18
73	STOP#	V10	106	CKE	N18
74	PAR	U10	107	MA7	V19
75	AD15	W11	108	MA8	V20
76	AD14	Y11	109	MA9	U18
77	AD13	V11	110	DQM7	T18
78	AD12	Y12	111	DQM6	T19
79	AD11	W12	112	DQM5	T20

Table 8-2 RAGE XL NAND Tree listing (BGA 256-pin package) (Continued)

Order	Signal Name	RAGE XL Pin Number	Order	Signal Name	RAGE XL Pin Number
113	WE#	R17	146	MD23	D17
114	DQM4	R18	147	MD24	D18
115	DQM3	R19	148	MD25	D19
116	DQM2	R20	149	MD26	D20
117	DSF	P17	150	MD27	C18
118	DQM1	P18	151	MD28	C19
119	DQM0	P19	152	MD29	C20
120	RAS#	P20	153	MD30	B20
121	HCLK	N20	154	MD31	A20
122	CAS#	L20	155	DFPCLK	M18
123	MD0	L18	156	MD32	B19
124	MD1	L19	157	MD33	A19
125	MD2	K18	158	MD34	B18
126	MD3	K19	159	MD35	A18
127	MD4	K20	160	MD36	C17
128	MD5	J18	161	MD37	B17
129	MD6	J19	162	MD38	A17
130	MD7	J20	163	MD39	C16
131	MD8	H18	164	MD40	B16
132	MD9	H19	165	MD41	A16
133	MD10	H20	166	MD42	C15
134	MD11	G17	167	MD43	B15
135	MD12	G18	168	MD44	A15
136	MD13	G19	169	MD45	D14
137	MD14	G20	170	MD46	C14
138	MD15	F17	171	MD47	B14
139	MD16	F18	172	MD48	A14
140	MD17	F19	173	MD49	D13
141	MD18	F20	174	MD50	C13
142	MD19	E17	175	MD51	B13
143	MD20	E18	176	MD52	A13
144	MD21	E19	177	MD53	D12
145	MD22	E20	178	MD54	C12

Table 8-2 RAGE XL NAND Tree listing (BGA 256-pin package) (Continued)

Order	Signal Name	RAGE XL Pin Number	Order	Signal Name	RAGE XL Pin Number
179	MD55	B12	184	MD60	A11
180	MD56	A12	185	MD61	C10
181	MD57	D11	186	MD62	B10
182	MD58	C11	output	MD63	A10
183	MD59	B11			

8.3 Test Modes

For the RAGE XL design, only one NAND tree is implemented connecting the digital pins; analog pins and power/ground pins are not considered in this test.

8.3.1 Board Test Modes

The RAGE XL chip enters one of the three board test modes by means of special-purpose “straps”. The pin named TESTEN is used to assert all required test modes. On the rising edge of TESTEN, the values on two input pins will be latched, as if they were straps. These two pins are ST0 and GNT#. All combinations of “strap” values are shown in the table below.

Table 8-3 Board Test Mode

ST0	GNT#	Board-test Mode
1	1	HIGH_Z
1	0	NAND_TREE
0	1	CHIP_ID
Others		Not for the NAND tree test

High-impedance Mode (HIGH_Z)

In this test mode, all bi-directional pins are forced to input direction, and all pure output pins (such as XTALOUT) are forced to high impedance.

NAND Tree Mode (NAND_TREE)

In this test mode, the vast majority of digital pins are connected to a lengthy, loop-sided chain of NAND gates. This mode is very similar to HIGH_Z mode: the digital pins are forced to input direction. The output (pin MD63) is forced to output direction.

Chip ID Mode (CHIP_ID)

This test mode is designed to identify the chip type and revision. Together, the 24 bits of CHIP_ID comprise a 16-bit “Device ID” and an 8-bit “Rev ID”. The IDs figured in this mode are identical to those provided by the register specification and accessible through normal software read operations.

Table 8-4 Information encoded by Rev ID

Bit	Rev ID							
	7	6	5	4	3	2	1	0
	c		b			a		
a	ASIC major revision number							
b	ASIC foundry							
c	ASIC minor revision number							

The 24 bits of CHIP_ID are in 4 multiplexed chunks on an 8-bit output data bus, MD[61:54]. The multiplexing selector signals are MD[53:50].

Table 8-5 Multiplexing selector signals for CHIP_ID

MD[61:54]	MD53	MD52	MD51	MD50
Device ID, upper-byte, [15:8]	1	0	0	0
Device ID, lower-byte, [7:0]	1	0	0	1
REV_ID, [7:0]	1	0	1	0

8.3.2 Other Test Modes

All remaining test modes are for ATI internal screening only, which includes several categories of “test vectors”

1. Scan test vectors (Internal Scan only; Boundary Scan is not supported).
2. Custom Memory test vectors (for the custom SRAMs in the chip).
3. Special test vectors (for the PLLs and DAC in the chip).
4. Functional test vectors (to catch the remaining defects which Scan cannot detect).

Over 97% of the flip-flops in the RAGE XL participate in the Internal Scan chains. This results in very high fault-coverage of the digital-logic portion of the chip. The custom SRAMs also benefit from a variety of DFT (Design For Testability), which results in 100% fault-coverage.

8.4 Testing Procedure

Initialization of the NAND tree test mode on RAGE XL is done in the following sequence:

- Set ST0 to 1 and GNT# to 0, also set TESTEN to 0.
- To set proper simulation configuration, MA0, MA6, and PCI33EN have to be set to 1
- After 200ns, set TESTEN to 1.This setting has to be kept until the test is finished
- After another 200ns, NAND tree test mode has been set properly: ST0, GNT#, MA0, MA6, PCI33EN, and other pins can be toggled according to the testing requirements and the test patter can be read on the output pin MD63.

NOTE: TESTEN has to be kept set to 1 during the test period.

8.5 Pins Unused in NAND Tree

- Power/ground and analog pins have been excluded from the NAND tree.
- The XTALIN and XTALOUT pins are not connected to the NAND tree, because both pins are tied to PLL circuitry which may be active during the RESET.

This page intentionally left blank.

Appendix A
Pin Listings

This appendix contains the pin listings for the RAGE XL.

To view the pin listing for the RAGE XL sorted by pin name, go to page *A-2*.

To view the pin listing for the RAGE XL sorted by pin number, go to page *A-6*.

A.1 Pins Sorted by Pin Name

Table A-1 Pins Sorted by Pin Name

BGA Pin Name	BGA Pin Number	BGA Pin Name	BGA Pin Number
AD0	V16	AD30	V2
AD1	W16	AD31	W1
AD2	V15	AD_STB0	W13
AD3	Y16	AD_STB1	Y4
AD4	W15	AGPCLAMP	U8
AD5	Y15	AS	J1
AD6	V14	AVDD	N4
AD7	W14	AVSSN	L4
AD8	Y14	AVSSQ	K4
AD9	V12	B	N1
AD10	Y13	BYTCLK	H1
AD11	W12	CAS#	L20
AD12	Y12	CBE0#	V13
AD13	V11	CBE1#	W10
AD14	Y11	CBE2#	Y8
AD15	W11	CBE3#	W4
AD16	V8	CKE	N18
AD17	W8	CPUCLK	V1
AD18	W7	CS0	W17
AD19	Y7	CS1	Y17
AD20	V7	DEVSEL#	Y10
AD21	Y6	DFPCLK	M18
AD22	W5	DFPDAT	V17
AD23	Y5	DQM0	P19
AD24	W3	DQM1	P18
AD25	Y3	DQM2	R20
AD26	V3	DQM3	R19
AD27	Y2	DQM4	R18
AD28	W2	DQM5	T20
AD29	Y1	DQM6	T19

Table A-1 Pins Sorted by Pin Name (Continued)

BGA Pin Name	BGA Pin Number	BGA Pin Name	BGA Pin Number
DQM7	T18	MA10	U19
DS	H2	MA11	U20
DSF	P17	MD0	L18
DVS0	D1	MD1	L19
DVS1	C1	MD2	K18
DVS2	C2	MD3	K19
DVS3	B2	MD4	K20
DVS4	A2	MD5	J18
DVS5	C3	MD6	J19
DVS6	B3	MD7	J20
DVS7	A3	MD8	H18
DVSCLK	E1	MD9	H19
FRAME#	W9	MD10	H20
G	M1	MD11	G17
GIOCLAMP	F4	MD12	G18
GNT#	T2	MD13	G19
HCLK	N20	MD14	G20
HSY	M2	MD15	F17
I2CCK	J2	MD16	F18
I2CDAT	J3	MD17	F19
INTR#	U3	MD18	F20
IRDY#	Y9	MD19	E17
LPVDD	B9	MD20	E18
LPVSS	A9	MD21	E19
MA0	Y18	MD22	E20
MA1	Y19	MD23	D17
MA2	Y20	MD24	D18
MA3	W18	MD25	D19
MA4	W19	MD26	D20
MA5	W20	MD27	C18
MA6	V18	MD28	C19
MA7	V19	MD29	C20
MA8	V20	MD30	B20
MA9	U18	MD31	A20

Table A-1 Pins Sorted by Pin Name (Continued)

BGA Pin Name	BGA Pin Number	BGA Pin Name	BGA Pin Number
MD32	B19	MONDET	E4
MD33	A19	MONID0	K1
MD34	B18	MONID1	K2
MD35	A18	MONID2	K3
MD36	C17	MONID3	J4
MD37	B17	N/C	B8, C8, C9, D5, D6, D2, M19, M20, R3, N19 U13, U17, U4, U5, V4
MD38	A17	PAR	U10
MD39	C16	PCI33EN	U16
MD40	B16	PVDD	L3
MD41	A16	PVSS	M4
MD42	C15	R	L1
MD43	B15	RAS#	P20
MD44	A15	REQ#	U1
MD45	D14	RESET#	U2
MD46	C14	ROMCS#	D3
MD47	B14	RSET	L2
MD48	A14	SAD0	G1
MD49	D13	SAD1	G2
MD50	C13	SAD2	G3
MD51	B13	SAD3	F2
MD52	A13	SAD4	F1
MD53	D12	SAD5	F3
MD54	C12	SAD6	E3
MD55	B12	SAD7	E2
MD56	A12	SB_STB	R1
MD57	D11	SBA0	N2
MD58	C11	SBA1	N3
MD59	B11	SBA2	P2
MD60	A11	SBA3	P3
MD61	C10	SBA4	P1
MD62	B10	SBA5	V5
MD63	A10	SBA6	W6

Table A-1 Pins Sorted by Pin Name (Continued)

BGA Pin Name	BGA Pin Number	BGA Pin Name	BGA Pin Number
SBA7	V6	TXCM	A7
SRDY	H3	TXCP	B7
ST0	T1	TXVDDR	C5, C7
ST1	T3	TXVSSR	A8, C4, C6
ST2	R2	VDDC	D8, L17, P4, U11
STOP#	V10	VDDP	T4, U14, U6, U9
TESTEN	U15	VDDR	D4, D7, D10, D16, G4, H17, K17, M17
TRDY#	V9	VREF	N17
TX0M	A6	VSS	D9, D15, H4, J9, J10, J11, J12, J17, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, R4, T17, U7, U12
TX0P	B6	VSY	M3
TX1M	A5	WE#	R17
TX1P	B5	XTALIN	A1
TX2M	A4	XTALOUT	B1
TX2P	B4		

A.1.1 Pins Sorted by Pin Number

Table A-2 Pins Sorted by Pin Number

BGA Pin Number	BGA Pin Name	BGA Pin Number	BGA Pin Name
A1	XTALIN	B13	MD51
A2	DVS4	B14	MD47
A3	DVS7	B15	MD43
A4	TX2M	B16	MD40
A5	TX1M	B17	MD37
A6	TX0M	B18	MD34
A7	TXCM	B19	MD32
A8	TXVSSR	B20	MD30
A9	LPVSS	C1	DVS1
A10	MD63	C2	DVS2
A11	MD60	C3	DVS5
A12	MD56	C4	TXVSSR
A13	MD52	C5	TXVDDR
A14	MD48	C6	TXVSSR
A15	MD44	C7	TXVDDR
A16	MD41	C8	N/C
A17	MD38	C9	N/C
A18	MD35	C10	MD61
A19	MD33	C11	MD58
A20	MD31	C12	MD54
B1	XTALOUT	C13	MD50
B2	DVS3	C14	MD46
B3	DVS6	C15	MD42
B4	TX2P	C16	MD39
B5	TX1P	C17	MD36
B6	TX0P	C18	MD27
B7	TXCP	C19	MD28
B8	N/C	C20	MD29
B9	LPVDD	D1	DVS0
B10	MD62	D2	N/C
B11	MD59	D3	ROMCS#
B12	MD55	D4	VDDR

Table A-2 Pins Sorted by Pin Number (Continued)

BGA Pin Number	BGA Pin Name	BGA Pin Number	BGA Pin Name
D5	N/C	G3	SAD2
D6	N/C	G4	VDDR
D7	VDDR	G17	MD11
D8	VDDC	G18	MD12
D9	VSS	G19	MD13
D10	VDDR	G20	MD14
D11	MD57	H1	BYTCLK
D12	MD53	H2	DS
D13	MD49	H3	SRDY
D14	MD45	H4	VSS
D15	VSS	H17	VDDR
D16	VDDR	H18	MD8
D17	MD23	H19	MD9
D18	MD24	H20	MD10
D19	MD25	J1	AS
D20	MD26	J2	I2CCK
E1	DVSCLK	J3	I2CDAT
E2	SAD7	J4	MONID3
E3	SAD6	J9	VSS
E4	MONDET	J10	VSS
E17	MD19	J11	VSS
E18	MD20	J12	VSS
E19	MD21	J17	VSS
E20	MD22	J18	MD5
F1	SAD4	J19	MD6
F2	SAD3	J20	MD7
F3	SAD5	K1	MONID0
F4	GIOCLAMP	K2	MONID1
F17	MD15	K3	MONID2
F18	MD16	K4	AVSSQ
F19	MD17	K9	VSS
F20	MD18	K10	VSS
G1	SAD0	K11	VSS
G2	SAD1	K12	VSS

Table A-2 Pins Sorted by Pin Number (Continued)

BGA Pin Number	BGA Pin Name	BGA Pin Number	BGA Pin Name
K17	VDDR	N19	N/C
K18	MD2	N20	HCLK
K19	MD3	P1	SBA4
K20	MD4	P2	SBA2
L1	R	P3	SBA3
L2	RSET	P4	VDDC
L3	PVDD	P17	DSF
L4	AVSSN	P18	DQM1
L9	VSS	P19	DQM0
L10	VSS	P20	RAS#
L11	VSS	R1	SB_STB
L12	VSS	R2	ST2
L17	VDDC	R3	N/C
L18	MD0	R4	VSS
L19	MD1	R17	WE#
L20	CAS#	R18	DQM4
M1	G	R19	DQM3
M2	HSY	R20	DQM2
M3	VSY	T1	ST0
M4	PVSS	T2	GNT#
M9	VSS	T3	ST1
M10	VSS	T4	VDDP
M11	VSS	T17	VSS
M12	VSS	T18	DQM7
M17	VDDR	T19	DQM6
M18	DFPCLK	T20	DQM5
M19	N/C	U1	REQ#
M20	N/C	U2	RESET#
N1	B	U3	INTR#
N2	SBA0	U4	N/C
N3	SBA1	U5	N/C
N4	AVDD	U6	VDDP
N17	VREF	U7	VSS
N18	CKE	U8	AGPCLAMP

Table A-2 Pins Sorted by Pin Number (Continued)

BGA Pin Number	BGA Pin Name	BGA Pin Number	BGA Pin Name
U9	VDDP	W3	AD24
U10	PAR	W4	CBE3#
U11	VDDC	W5	AD22
U12	VSS	W6	SBA6
U13	N/C	W7	AD18
U14	VDDP	W8	AD17
U15	TESTEN	W9	FRAME#
U16	PCI33EN	W10	CBE1#
U17	N/C	W11	AD15
U18	MA9	W12	AD11
U19	MA10	W13	AD_STB0
U20	MA11	W14	AD7
V1	CPUCLK	W15	AD4
V2	AD30	W16	AD1
V3	AD26	W17	CS0
V4	N/C	W18	MA3
V5	SBA5	W19	MA4
V6	SBA7	W20	MA5
V7	AD20	Y1	AD29
V8	AD16	Y2	AD27
V9	TRDY#	Y3	AD25
V10	STOP#	Y4	AD_STB1
V11	AD13	Y5	AD23
V12	AD9	Y6	AD21
V13	CBE0#	Y7	AD19
V14	AD6	Y8	CBE2#
V15	AD2	Y9	IRDY#
V16	AD0	Y10	DEVSEL#
V17	DFPDAT	Y11	AD14
V18	MA6	Y12	AD12
V19	MA7	Y13	AD10
V20	MA8	Y14	AD8
W1	AD31	Y15	AD5
W2	AD28	Y16	AD3

Table A-2 Pins Sorted by Pin Number (Continued)

BGA Pin Number	BGA Pin Name	BGA Pin Number	BGA Pin Name
Y17	CS1	Y19	MA1
Y18	MA0	Y20	MA2

Appendix B
Revision History

Note: Naming of Rev 2.0 to 2.4 did not conform to the release naming convention. They have been renamed Rev 0.1 to 0.5 respectively.

Oct. 1998: GCS-C04300 Rev 0.01 (GC43001.pdf)

Initial document.

Oct. 1998: GCS-C04300 Rev 0.02 (GC43002.pdf)

Change in name of product.

Nov. 1998: GCS-C04300 Rev 0.03 (GC43003.pdf)

Corrections in the pinout consistency for the PQFP-type package.

Nov. 1998: GCS-C04300 Rev 0.04 (GC43004.pdf)

Updated Table 3-28.

Jan. 1999: GCS-C04300 Rev 0.05 (GC43005.pdf)

Updated pinout (pad #138 in PQFP).

Mar. 1999: GCS-C04300 Rev 0.06 (GC43006.pdf)

Compared and reviewed all aspects of this document with the engineering specifications (Rage XL/XC Pinout Specification Rev. 1.16).

- Reworked Appendix A (Pin Listings).
- Added Chapters 2-1 and 2-2.
- Chapter 3.1: Pin Summary, Table 3-1: Pin Summary by Functional Group. Corrected pin count.

- Chapter 3.2: Pin Out Fig 3-2: RAGE XL Top View
  Corrected pin descriptions (removed VPP and replaced with VDDP, removed AVSS and replaced with AVSSQN and AVSSQ).
- Chapter 3.3: Host Bus Interface, Table 3-2: AGP/PCI Host Bus Interface
  Cleaned up the descriptions.
- Chapter 3.4: Video Memory Interface, Table 3-4: Video Memory Interface
  Consolidated MD[63:32]
- Chapter 3.4: Video Memory Interface, Table 3-5: 64-bit Wide Memory
  Added 32Mbit SGRAM and 64 Mbit SDRAM. Cleaned up table.
- Chapter 3.4: Video Memory Interface, Table 3-6: 32-bit Wide Memory
  Added 64 Mbit SDRAM. Cleaned up table.
- Chapter 3.4: Video Memory Interface, Table 3-7: Memory Mapping
  Added SGRAM (DIMM) 512Kx32x2 (32Mb) and SDRAM 1Mx32x2 (64Mb). Cleaned up table.
- Chapter 3.4: Video Memory Interface, Table 3-8: BIOS Memory Mapping
  Cleaned up table.
- Chapter 3-5: Multimedia Interface, Table 3-10: Standard Multimedia Configurations
  Added to the note to bottom of the table. Cleaned up table.
- Chapter 3-11: Differences in Pinouts: Table 3-29: RAGE Mobility vs RAGE XL Differences.
  Added new table.
- Chapter 3-10: Configurations for the Strap/BIOS Implementation, Configuration #1: For add-in card designs.
  Added new description at the of numbered list.
- Chapter 3-10: Configurations for the Strap/BIOS Implementation, Configuration #2: For motherboard designs.
  Added new description at the of numbered list.
- Chapter 3-10: Configurations for the Strap/BIOS Implementation, Configuration #3: Combination of 1 and 2.
  Added new description.
- Chapter 3-10: Configurations for the Strap/BIOS Implementation, Table 3-22: ROM BIOS Straps.
  Updated entire table.
- Chapter 6-1: Electrical Characteristics, Calculating RSET Resistance (DAC Interface).
  Updated the vaule of the RSET resistor and the derived calculation for RSET.

Apr. 1999: GCS-C04300 Rev 0.07 (GC43007.pdf)

- General edits.
- Chapter 2-3: General Features
  150 MHz, in 4MB and 8MB support, has been changed to 143 MHz.
- Chapter 2-4-3: LCD Panel Support
  Added Portrait mode support.
- Chapter 2-4-4: ACPI Power Management
  Added self-refreshed SDRAM/SGRAM in Suspend Mode.
- Chapter 2-4-7: Memory Support
  Changed all.
- Chapter 3-1: Pinout Summary
  Changed pincount for CRT Monitor from 8 to 9 pins.
- Chapter 3-4: Video Memory Interface
  Removed Tables 3-5, 3-6 and 3-7. The tables are moved to Chapter 4-9-3 (see below).
- Chapter 4-3-3: Display Controller
  Removed reference to FIFO #2.
- Chapter 4-5: Chip Power Management
  Replaced reference to 5.0 V with 2.5 V as an operation condition.
- Chapter 4-9-3: Memory Controller and Interface/Memory Interface Mapping
  Memory Interface information is moved here from “Pinout” chapter.
  Memory Type and Configuration Tables for 64-bit and 32-bit wide memory are updated and moved here from “Pinout” chapter.
  Added Figure 4-7 “SDRAM Implementation (16 Mbit) - RGAE XC”.
  Updated Figure 4-6 “SDRAM Implementation (16 Mbit) - RGAE XL” and Figure 4-13 “AMC Interface”.
- Chapter 5-3: TMDS Timing
  Removed all TFT tables.
- Chapters 6-2-1 and 6-2-2: Thermal Characteristics/Maximum Ambient Temperature and Maximum Recommended Junction and Case Temperature
  Reorganized the content. Updated with the latest test results.
- Chapters 6-1-5: Input/Output Specifications
  Added Table 6.10 Transmitter Electrical Specifications.

- Chapter 6-2-3: Thermal Characteristics/Power Consumption and Case Temperature Measurements
  Reorganized the content. Updated with the latest test results.
- Appendix A: Pin Assignment Tables
  All 4 tables are redone for most efficient use of the page space.
- Added new Chapter 8: NAND Tree Implementation.
- Changed maximum TFT display mode to 1024x780.

July 1999: GCS-C04300 Rev 0.08 (GC43008.pdf)

- Reformatted Tables 4-1 and 4-2, and edited text in the same section (4.9.1).
- Added 512Kx32x4 memory support in section 4.9 and in Table 4-2.
- Removed 1Mx32x2 memory support from section 4.9 and from Table 4-2.
- Removed SSTL support. Chapter 3, pages 3-1 and 3-21 under Vref description.

Aug 1999: GCS-C04300 Rev 1.00 (GC43100.pdf)

- Modified Table 3-7 to include ZV port Video Capture support.
- Modified Table 3-23 to include ZV port support.
- Modified Table 3-27 to include ZV port support.

Above changes to reflect additional features in chip rev B31

Nov 1999: GCS-C04300 Rev 1.01 (GC43101.pdf)

- Added an XL/XC feature summary to beginning of Chapter 2.
- Chapter 2-1: General features:
  Modified “Supports 2MB to 8MB SGRAM at up to 125 MHz ... higher memory speeds” to “Supports flexible memory configurations from 4 MB to 8 MB SDRAM/SGRAM ... 64-bit interface.”
  Modified “Supports 4 MB 1Mx16 SDRAM and 8 MB 2Mx32... lowest cost configurations” to “Supports 4 MB 1Mx16 or 8 MB 2Mx32 SDRAM at up to ... lowest cost configurations”.
  Removed “Supports 8 MB SDRAM at up to 143 MHz across 64-bit interface”.
  Added “Memory upgrade via industry standard ... higher memory speeds”.
- Chapter 2-3-1: Feature Compatibility with RAGE 128 VR
  Removed “Supports potrait mode” and “Supports front-end alpha blending...”.
- Chapter 2-4-2: Digital Flat Panel Support (Not RAGE XC)
  Removed “Portrait mode support for accelerated modes without overlay”,

"Programmable internal timer for automatic power down of panel" and "Power Up/Down Sequencer".

- Chapter 2-4-4: AGP 2X Mode
  Removed.
- Chapter 2-4-6: Memory Support
  Modified "Support for both LVTTL and SSTL memory interface" to "Support only LVTTL".
- Chapter 2-4-7: DVD and Video Support (Not RAGE XC)
  Added "Support 4-bit video and graphics alpha blending ARGB8888...".
- Chapter 2-4-10: Motion Video Acceleration
  Removed.
- Chapter 2-4-11: AMC Support (Not RAGE XC)
  Changed 16-bit to 8 bit.
- Chapter 2-5: Software Features
  Merged columns Win 95 and Win 98 into column Win9x.
- Chapter 3-1: Pinout Summary
  Removed functional group LVTTL (VREF). Changed group I/O Power (VDDR) to include VREF (i.e. I/O Power (VDDR) + VREF), and the corresponding pin count for Rage XL BGA-type Package to 9. Changed pin-count for I/O Ground (VSSR) from 15 to 16 and changed pin-count from PCI/AGP Ground (VSSP) from 4 to 3.
- Fig. 3-1, 3-2, Table 3-2, 3-3, Fig. 4-3:
  Changed ADST# to AD_STB and SBST# to SB_STB.
- Table 3-17: Power and Ground Pins
  Changed pin count for VDDC, VDDP, VDDR, and VSS. Added signals LPVDD, LPVSS, TXVDDR, and TXVSSR.
- Table 3-18: External Straps
  Reordered rows in the table. Rows now ordered by pin name.
- Table 3-21: Chip ID
  Removed rows with Bus Interface AGP test Mode and PCI 33 MHz, 5.0V signaling.
- Table 3-23: Function Support Differences: RAGE XL vs RAGE 128
  Changed B31 to B41.
- Table 3-25: Function Support Differences: RAGE XL vs RAGE PRO
  Modified "Supports alpha blending ARGB4888" to "Supports video and graphics alpha blending ARGB8888"
  Removed row for Portrait Mode function.
- Table 3-27: Feature Comparison: Rage XL vs RAGE Mobility
  Changed B31 to B41.

- Figure 4-1: Rage XL Function block Diagram
  Removed mach64 2D Engine from Display Controller; added Video/Graphics Alpha Blender block, DVD Subpicture block and CRT DAC block and removed Hardware Icon block.
- Chapter 4-1 (2D Engine) and 4-2 (3D Graphics Coprocessor)
  Changed order.
- Chapter 4-4-2: CRT Controller
  Changed screen resolutions from 1600x1200 to 1920x1080.
- Chapter 4-4-3: Display Controller
  Changed description of display controller.
- Chapter 4-4-7: Palette DAC
  Section is now Palette and CRT DAC
  Changed resolutions from 1600x1200 to 1920x1080.
- Chapter 4-4-10: Ratiometric Expansion (Not in XC)
  Instead of just indicating “Ratiometric expansion uses two algorithms”, specified the algorithms “replication or blending”.
- Fig. 4-5 SDRAM Implementation (16 Mbit) - RAGE XL, and Fig. 4-6 SDRAM Implementation (16 Mbit) - RAGE XC
  Removed (AP), and changed A(11:0) to A(9:0), A10/AP, and A11/BS.
- Fig. 4-9 SGRAM Implementation (32 Mbit)
  Changed right side of diagram (512Kx32x2 SGRAM) to be the same as RAGE Mobility-128.
- Fig. 4-10 SDRAM Implementation (64 Mbit)
  Removed (AP).
  Changed A(10:0) to A(9:0) and A10/AP.
- Section 8.3.1 Order of NAND tree connection
  Changed “There is only one NAND tree in RAGE XL” to “There is only one NAND tree in RAGE XC”.

Dec 1999: GCS-C04300 Rev 2.00 (GC43200.pdf)

- Removed all references and material related to RAGE XC.
- Corrected Figure 4-7 (4-8 in previous version).
- Replaced ZV by ITU-601 in Table 3-7.

Mar 2000: GCS-C04300 Rev 2.01 (GC43201.pdf)

- Modified VREF description in Table 3-25.

- Corrected typo in Table 3-17. Number of pins for VDDC and VDDP changed to 4 and 4 instead of 5 and 3.
- Changed PC 98 compliant to PC 99 compliant on page 2-1.
- Corrected cell entries in Fig 3-1:
  - T4 changed to VDDP instead of VPP.
  - W4 changed to CBE3# instead of CBE#3.
  - Y8 changed to CBE2# instead of CBE#3.
  - V13 changed to CBE0# instead of CBE#0.
  - In H18, H19, J18 to J20, K18 to K20, and L18 to L19, "0" was dropped.
- Table 3-2 APG/PCI Bus Interface, page 3-3:- signal names CBE#[3:0] changed to CBE[3:0]#.
- Table 3-7 Standard Multimedia Configurations, page 3-7:- signal names SDA and SCL changed to I2CDAT and I2CCK, respectively.
- Table A-1:- Added the following missing entries to the list: VREF, N/C (N19), SBA$ and SBA6.
- Table A-2 Pins sorted by pin number, page A-9:- BGA pin name M09 changed to MA9.

Apr 2000: GCS-C04300 Rev 2.02 (GC43202.pdf)

- Changed SXGA to XGA support in section 5.3.1.
- Modified notes on the AGPCLAMP and GIOCLAMP descriptions in Table 3-14.

Oct 2000: GCS-C04300 Rev 2.03 (GC43203.pdf)

- Changed section 6.2.3 to show new power and thermal data of ASIC version B41.
- Table 3-4: updated description of DSF.
- Table 3-2: rectified pin type for SBA7/IDSEL and SB_STB to I/O and O respectively.
- Modified Table 6-9 extensively.

Nov 2001: CHS-R3L-00-30 (CHS-R3L-00-30.pdf)

- General edits. Clarified that RAGE XL supports both PCI-33 and PCI-66 modes (in addition to AGP).

Sep 2003: CHS-R3L-00-31 (CHS-R3L-00-31.pdf)

- Clarified statement on the requirement of external straps in section 3.10.
- Updated Table 6-9: Changed PU to PD for CAS#, MA[11:0], and MD[63:0]; added 50K PU for DVS[7:0]; added a note on the requirement of external straps.

Dec 2003: CHS-R3L-00-32 (CHS-R3L-00-32.pdf)

- Added Table 6-13 RAGE XL Thermal Characteristics.